

Fleet: CORE_B Reference Schematic (A02)
for Magellan and Columbus
REV : 2.2 2014-06-27

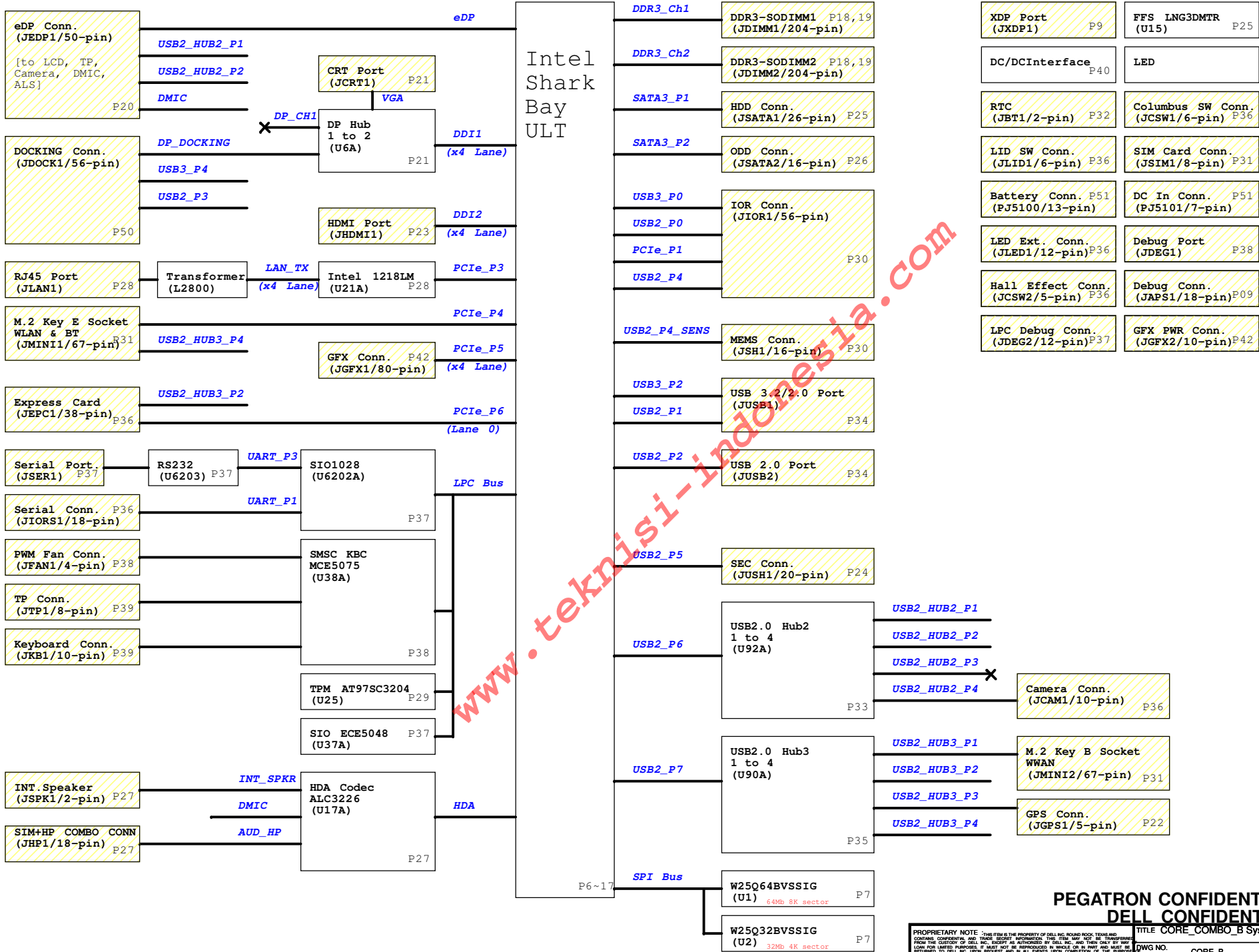
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DWG NO.	CORE_B	REV.	2.2
DATE	Thursday, September 18, 2014	SHEET	1 of 65



CORE_COMBO_B System Block Diagram (A02)



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CORE_COMBO_B Index and Conf i gur at on(A02)

USB2.0 Port Map Configurati o

HSW ULT	USB2.0	Schematic Confi gur at b	Dest i nati o
	0	USB2_P0	JIOR1-->IOR_M-->Right
	1	USB2_P1	JUSB1-->MB-->Lef t
	2	USB2_P2	JUSB2-->MB-->Back
	3	USB2_P3	JDOCK1-->DOCK
	4	USB2_P4	JIOR1,JSH1 -->Co-layout
	5	USB2_P5	JUSH1-->USH->SC, RFID, FPR
	6	USB2_P6	HUB2-->TSC, WebCam, Reserved, Camera
	7	USB2_P7	HUB3-->WWAN, Exp/PC, GPS, WLAN

USH Configurati o

USH	0	BIO
	1	NA

POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALW PLANE	M PLANE	SUS PLANE	RUN PLANE	CLK
S0 (Full ON) with M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) with M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) with M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) with M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) with M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) with M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) with M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCIe/USB3.0/SATA Port Map Configurati o

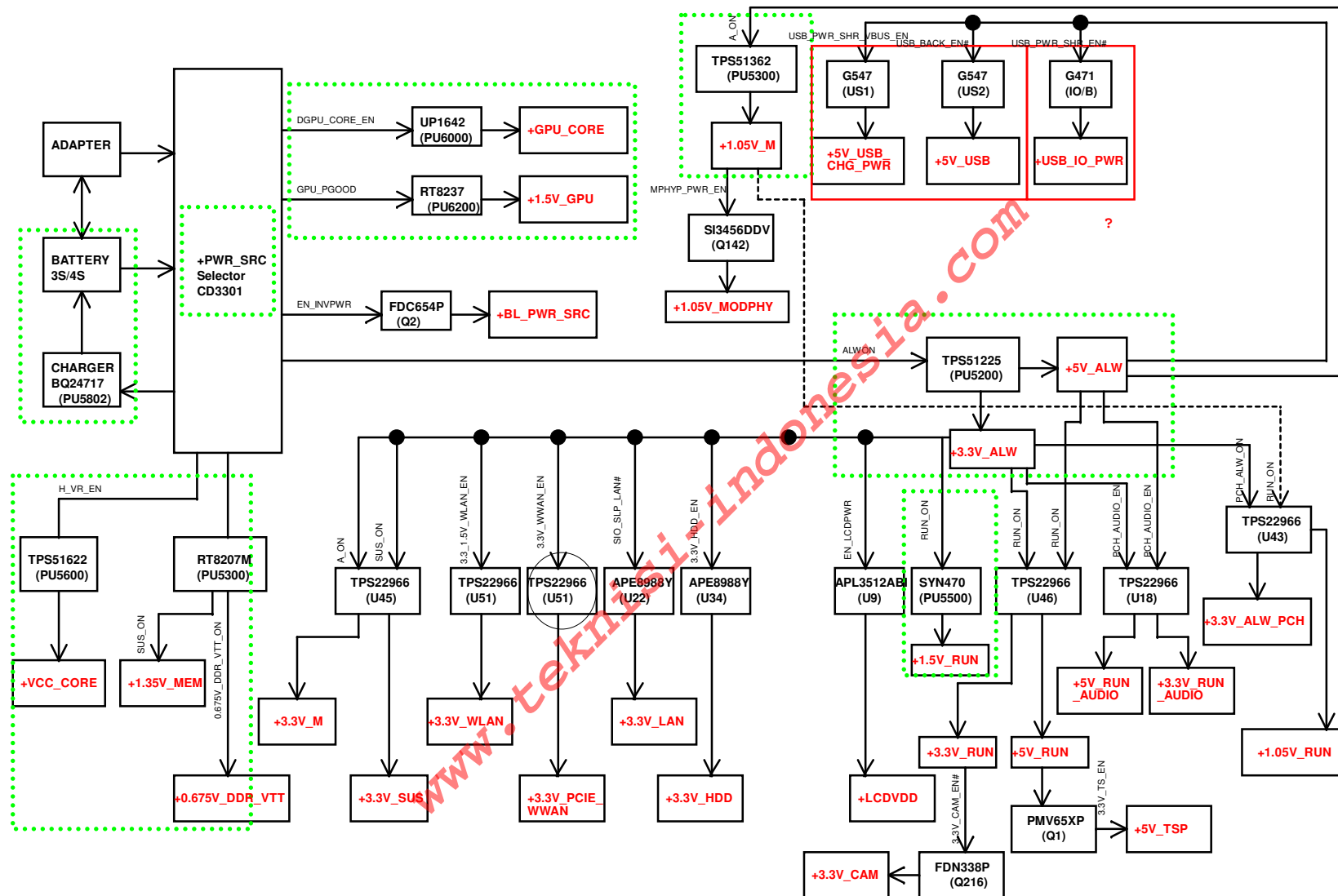
PCI E	USB3.0	SATA	Schematic Confi gur at b	Dest i nati o
	USB3.0 1		USB3_P0	JIOR1-->IO-->Right
	USB3.0 2		USB3_P1	JUSB1-->MB-->LEFT
PCIE 1	USB3.0 3		PCIE_P1	JIOR1-->IO-->Right
PCIE 2	USB3.0 4		USB3_P3	JDOCK1-->DOCK
PCIE 3			PCIE_P3	LOM
PCIE 4			PCIE_P4	JMINI1-->WLAN (WiGi)
PCIE 5			PCIE_P5	JGFX1-->GPX BD
PCIE 6		SATA 3	PCIE_P6	JEPC1-->Express/PC Card
		SATA 2	SATA3_P2	ODD
		SATA 1	SATA3_P1	HDD
		SATA 0	NA	N/A

PM TABLE

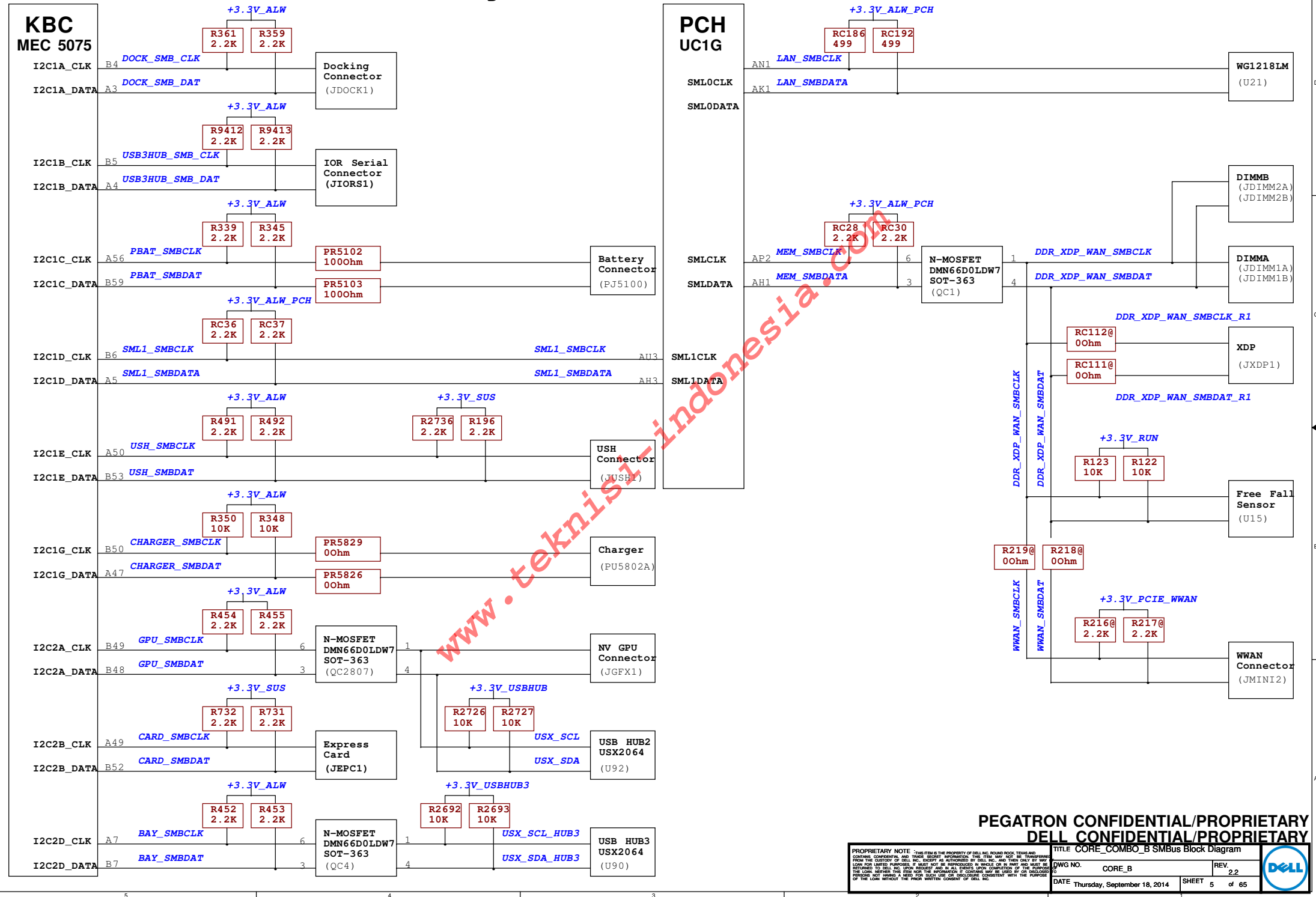
power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/No AC	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

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CORE_COMBO_B SMBus Block Diagram (A02)



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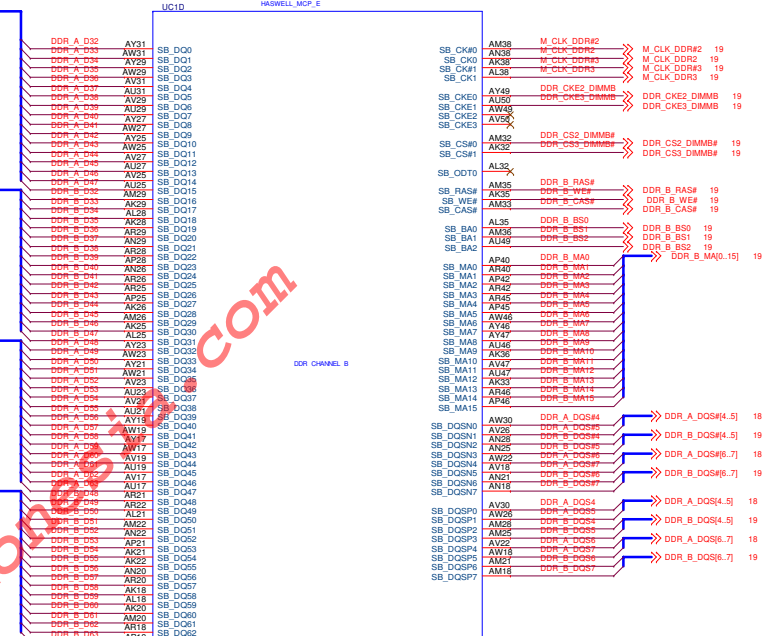
DDR interleave routing



0101-01SX0DE

Rev1p2

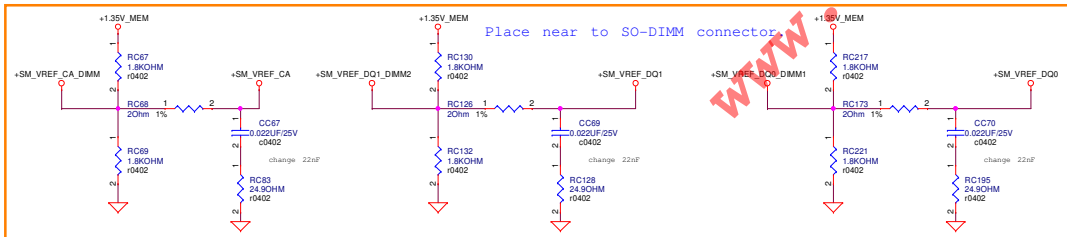
DDR interleave routing



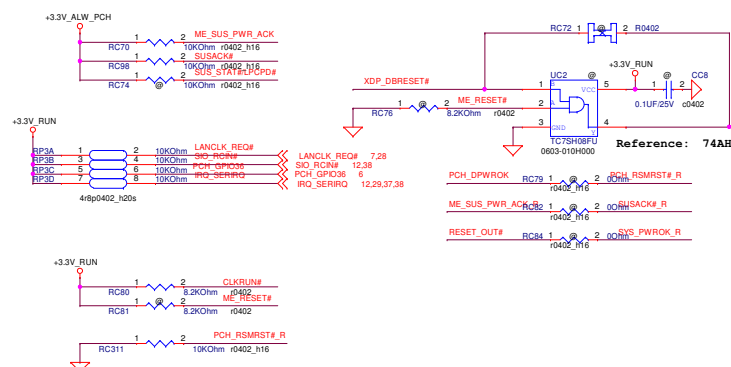
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Interleaved Memory

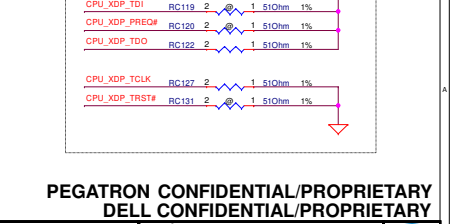
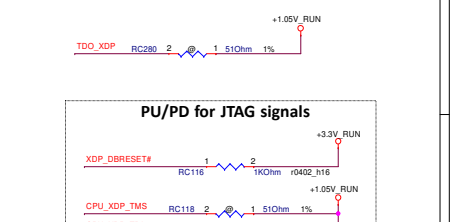
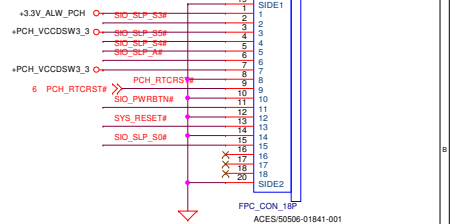
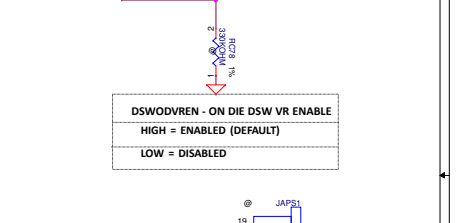
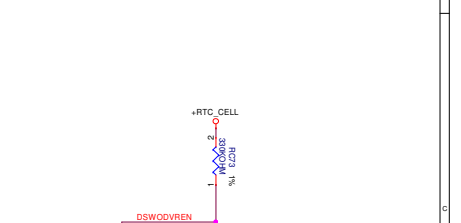
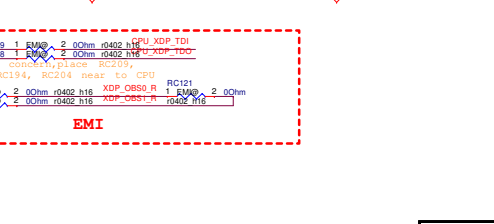
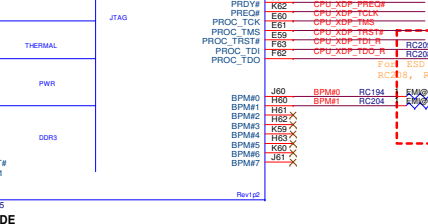
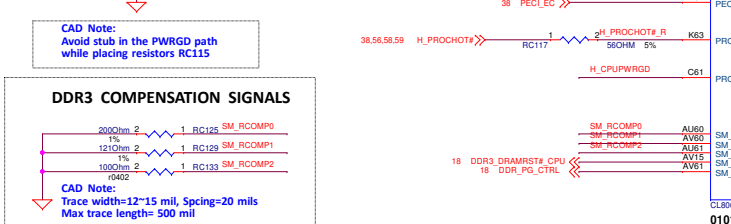
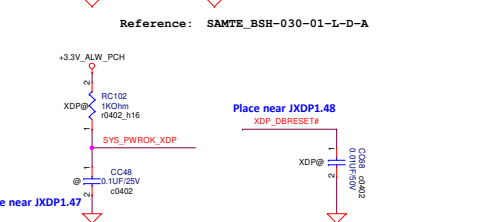
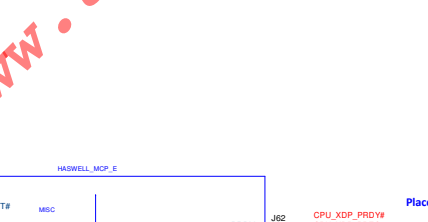
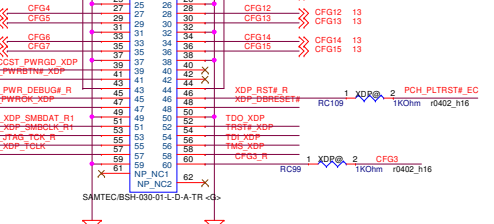
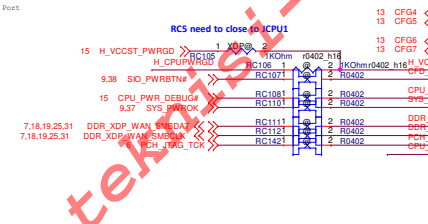
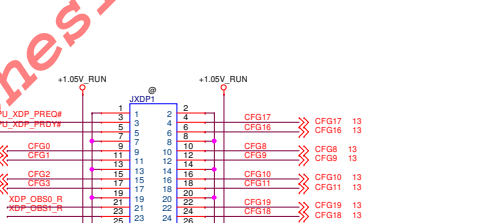
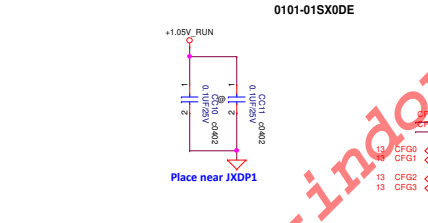
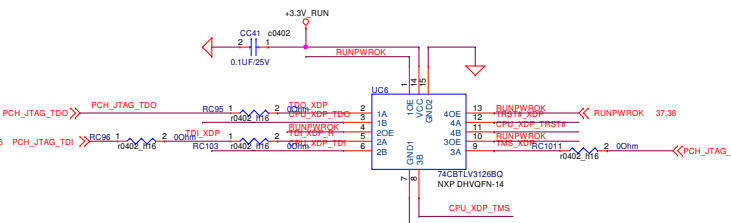
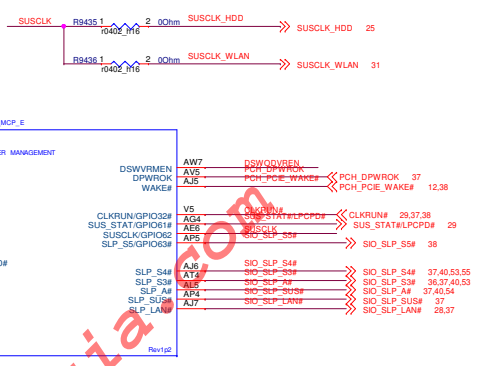
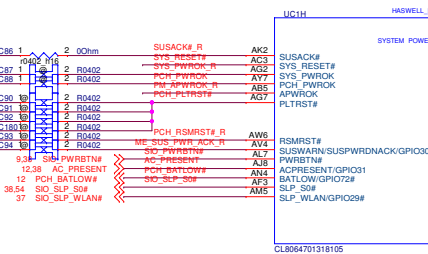
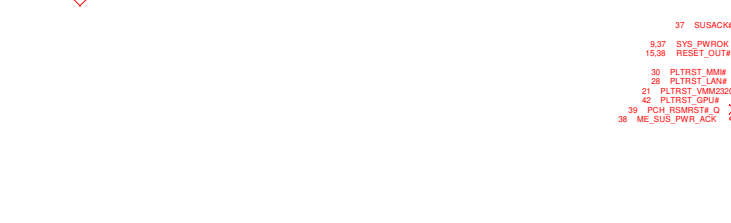
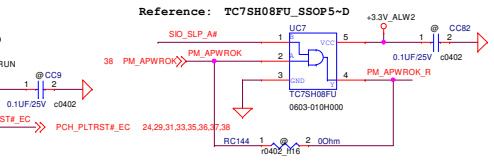
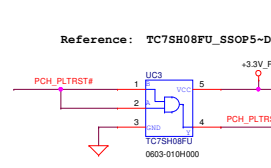


Refer to Intel request PDG1.0 P148

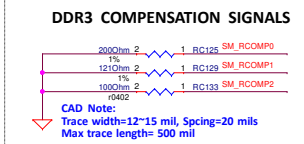


DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86, R319, RC267	RC79, RC82, RC265
Depop	RC79, RC82, RC265	RC86, R319, RC267



CAD Note:
Avoid stub in the PWGRD path
while placing resistors RC115



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Place near JXDPI.47

Place near JXDPI.48

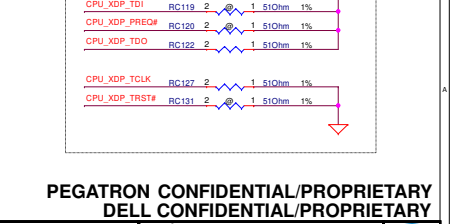
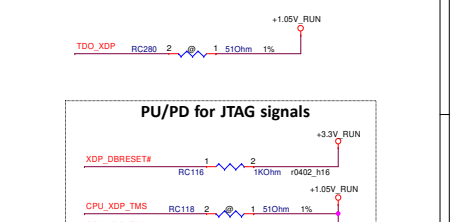
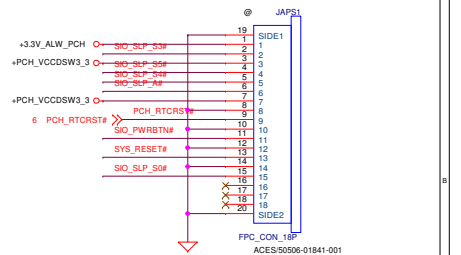
Place near JXDPI.49

Place near JXDPI.50

Place near JXDPI.51

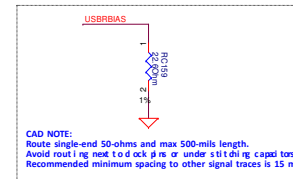
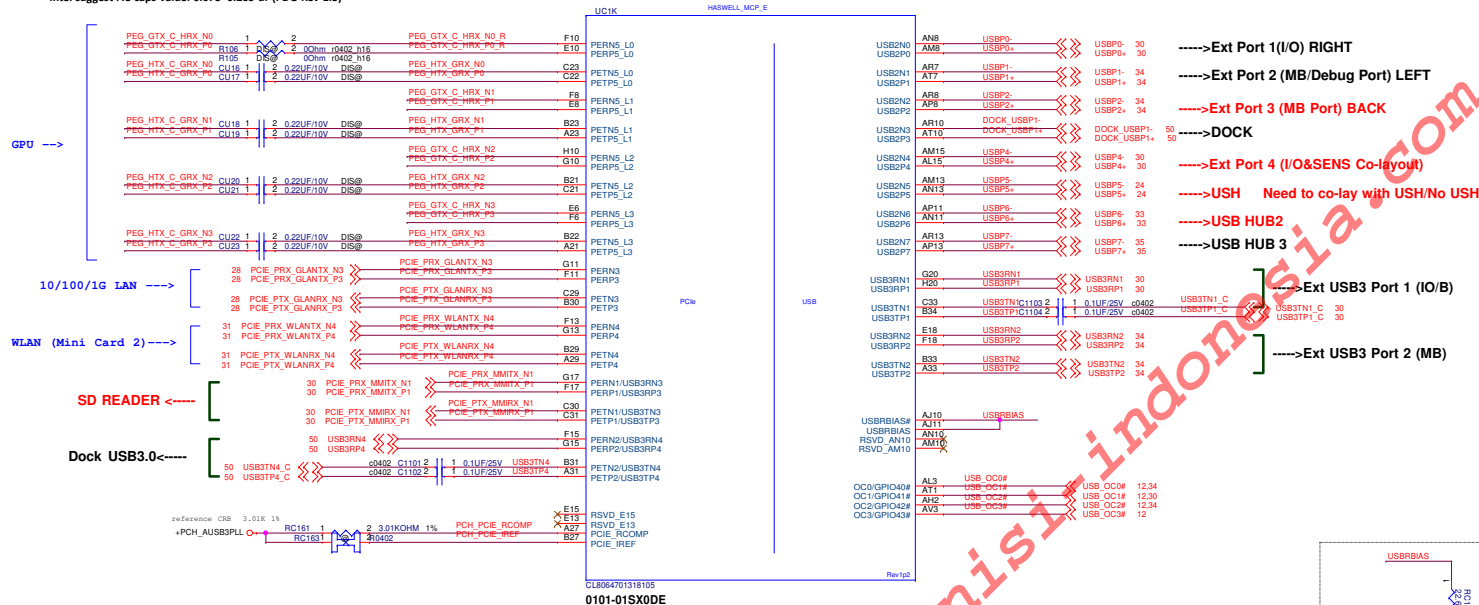
Place near JXDPI.52

DSWVDREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED



42 PEG_GTX_C_HRX_N0_3] PEG_GTX_C_HRX_N0_3]
42 PEG_GTX_C_HRX_P0_3] PEG_GTX_C_HRX_P0_3]
42 PEG_HTX_C_GRX_N0_3] PEG_HTX_C_GRX_N0_3]
42 PEG_HTX_C_GRX_P0_3] PEG_HTX_C_GRX_P0_3]

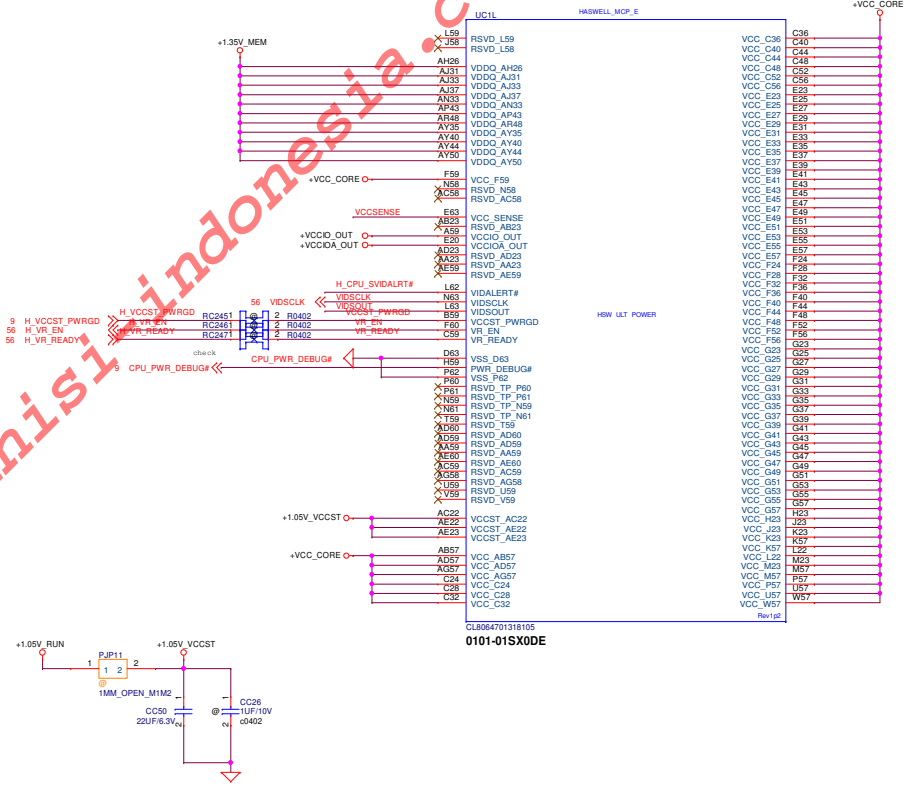
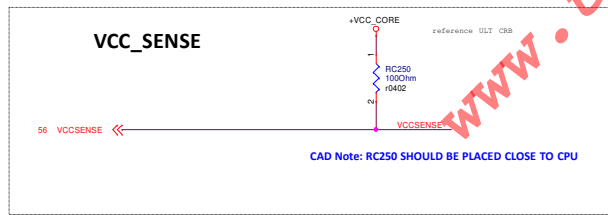
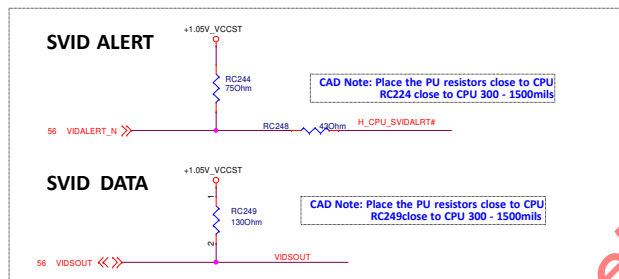
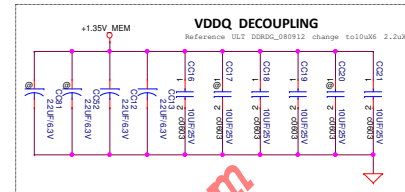
AC caps follow nV suggest i on mdffy to 0.22uF
Intel suggest AC caps value: 0.075~0.265 uF (PDG Rev 1.5)



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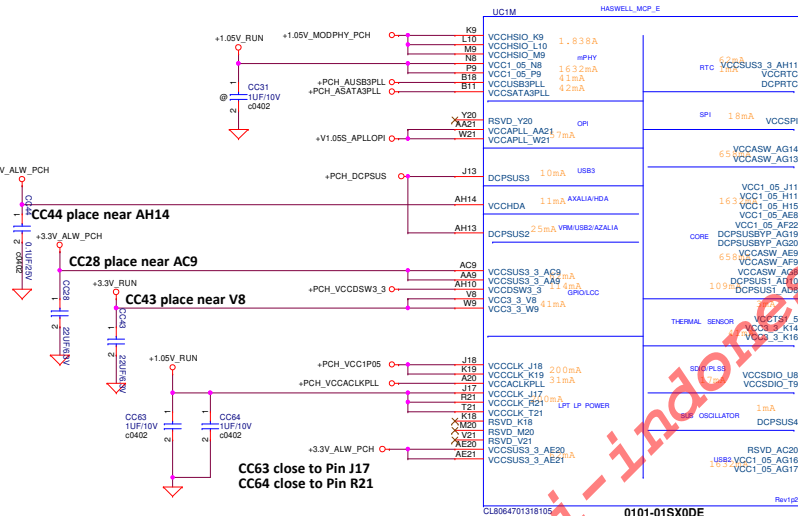
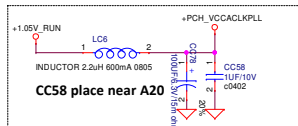
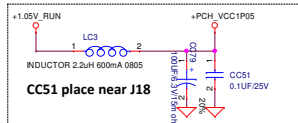
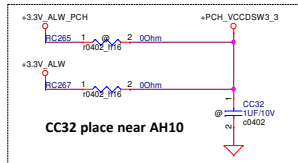
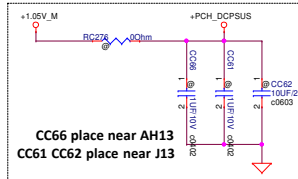
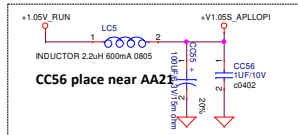
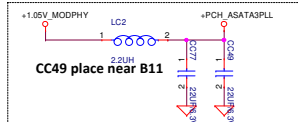
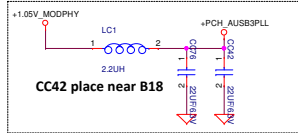
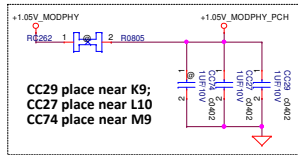
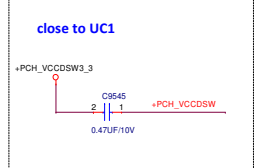
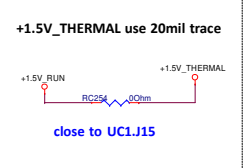


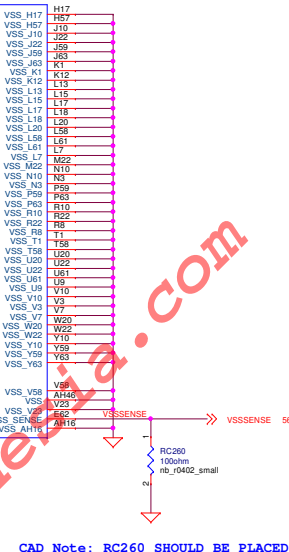
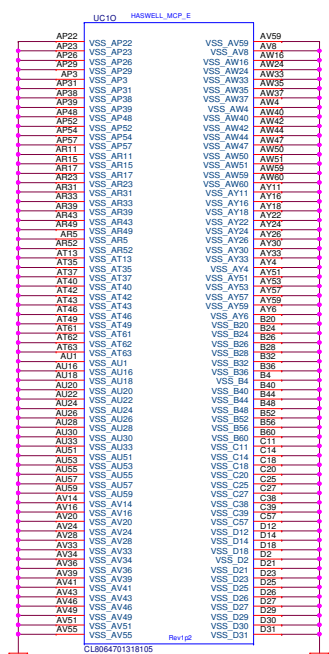
Table 6-3. Pre-Si I_{CC}max Estimates

Voltage Rail	Voltage (V)	S0 I _{CC} max Current (A)	Sx I _{CC} max Current (A)	Deep Sx I _{CC} max (A)	G3
VCC1_05	1.05	1.741	0	0	0
VCC1_05 (Internal Suspend VR mode using INTRVREN)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.097	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCSATA3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCC1S1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCSDA	3.3	0.011	0	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTRVREN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTRVREN)	3.3	0.062	0.005	0	0
DcpSus1 ¹	1.05	0.109	0.014	0	0
DcpSus2 ²	1.05	0.025	0.001	0	0
DcpSus3 ³	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μ A See notes 1, 2

DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86, R319, RC267	RC79, RC82, RC265
Depop	RC79, RC82, RC265	RC86, R319, RC267





CAD Note: RC260 SHOULD BE PLACED CLOSE TO CPU

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Rev1p2

CL8064701318105

0101-01S3X0DE

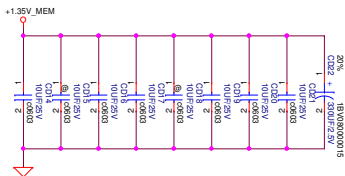
Rev1p2

CL8064701318105

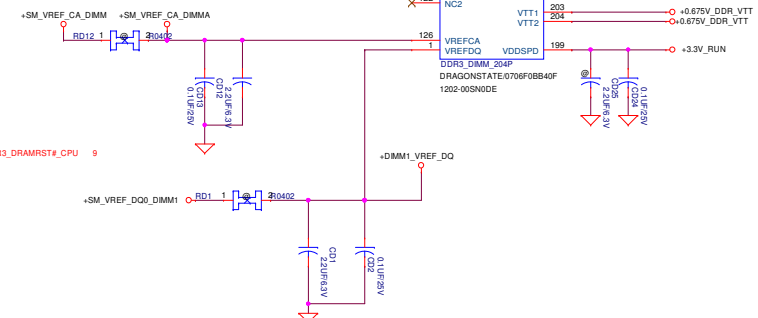
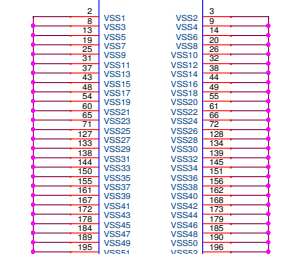
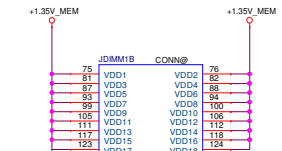
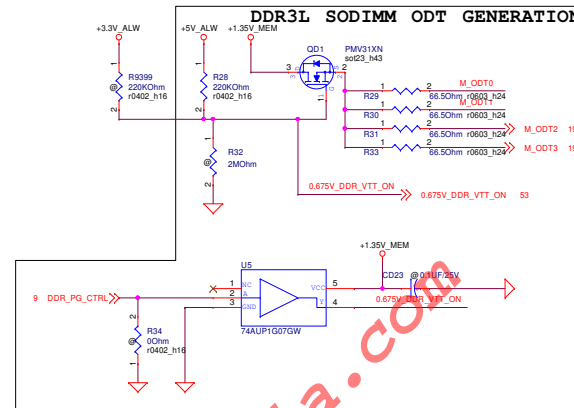
CAD Note: RC260 SHOULD BE 1

```
8 DDR_A_DQS#[0..7] <<>>
8 DDR_A_D[0..63] <<>>
8 DDR_A_DQS[0..7] <<>>
8 DDR_A_MA[0..15] >>
```

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



		CON@N	
DOR_A_MAO	98	DDMA1	4
DOR_A_MSA1	97	A0	DOR_A_D0
DOR_A_MSA2	96	A1	DOR_A_D1
DOR_A_MSA3	95	A2	DOR_A_D2
DOR_A_MSA4	94	A3	DOR_A_D3
DOR_A_MSA5	93	A4	DOR_A_D4
DOR_A_MSA6	90	A5	DOR_A_D5
DOR_A_MSA7	86	A6	DOR_A_D6
DOR_A_MSA8	87	A7	DOR_A_D7
DOR_A_MSA9	88	A8	DOR_A_D8
DOR_A_MSA10	89	A9	DOR_A_D9
DOR_A_MSA11	84	A10/AP	DOR_A_D10
DOR_A_MSA12	83	A11	DOR_A_D11
DOR_A_MSA13	81	A12/BCB	DOR_A_D12
DOR_A_MSA14	79	A13	DOR_A_D13
DOR_A_MSA15	78	A14	DOR_A_D14
		A15	DOR_A_D15
			DOR_A_D16
M_CLK_DOR1	102	CK1	DOR_A_D17
M_CLK_DOR2	101	CK1#	DOR_A_D18
M_CLK_DOR3	100	CK0	DOR_A_D19
M_CLK_DOR4	103	CK0#	DOR_A_D20
DOR_CS1_DDMA0A	121	S1#	DOR_A_D21
DOR_CS2_DDMA0B	118	S0#	DOR_A_D22
			DOR_A_D23
			DOR_A_D24
M_GDT1	116	QD29	DOR_A_D25
M_GDT2	114	QD28	DOR_A_D26
		QD27	DOR_A_D27
		QD26	DOR_A_D28
DOR_A_WE#	110	WE#	DOR_A_D29
DOR_A_RAS#	113	CAS#	DOR_A_D30
DOR_A_CAS#	112		DOR_A_D31
			DOR_A_D32
DOR_A_BS2	79	BA2	DOR_A_D33
DOR_A_BS1	108	BA1	DOR_A_D34
DOR_A_BS0	109	BA0	DOR_A_D35
DOR_CKE1_DDMA	73	CKE1	DOR_A_D36
DOR_CKE2_DDMA	74	CKE2	DOR_A_D37
			DOR_A_D38
			DOR_A_D39
			DOR_A_D40
			DOR_A_D41
			DOR_A_D42
			DOR_A_D43
			DOR_A_D44
			DOR_A_D45
			DOR_A_D46
			DOR_A_D47
			DOR_A_D48
			DOR_A_D49
			DOR_A_D50
			DOR_A_D51
			DOR_A_D52
			DOR_A_D53
			DOR_A_D54
			DOR_A_D55
			DOR_A_D56
			DOR_A_D57
			DOR_A_D58
			DOR_A_D59
			DOR_A_D60
			DOR_A_D61
			DOR_A_D62
			DOR_A_D63
			DOR_A_D64
			DOR_A_D65
			DOR_A_D66
			DOR_A_D67
			DOR_A_D68
			DOR_A_D69
			DOR_A_D70
			DOR_A_D71
			DOR_A_D72
			DOR_A_D73
			DOR_A_D74
			DOR_A_D75
			DOR_A_D76
			DOR_A_D77
			DOR_A_D78
			DOR_A_D79
			DOR_A_D80
			DOR_A_D81
			DOR_A_D82
			DOR_A_D83
			DOR_A_D84
			DOR_A_D85
			DOR_A_D86
			DOR_A_D87
			DOR_A_D88
			DOR_A_D89
			DOR_A_D90
			DOR_A_D91
			DOR_A_D92
			DOR_A_D93
			DOR_A_D94
			DOR_A_D95
			DOR_A_D96
			DOR_A_D97
			DOR_A_D98
			DOR_A_D99
			DOR_A_D100
			DOR_A_D101
			DOR_A_D102
			DOR_A_D103
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			DOR_A_D105
			DOR_A_D106
			DOR_A_D107
			DOR_A_D108

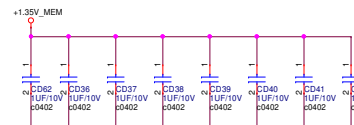


CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN

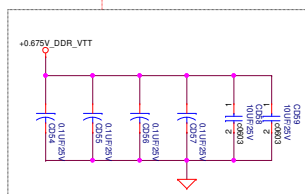
8 DDR_B_DQS#[0..7] <<>>
8 DDR_B_D[0..63] <<>>
8 DDR_B_DQS[0..7] <<>>
8 DDR_B_MA[0..15] >>

Layout Note:
Place near JDIMM1

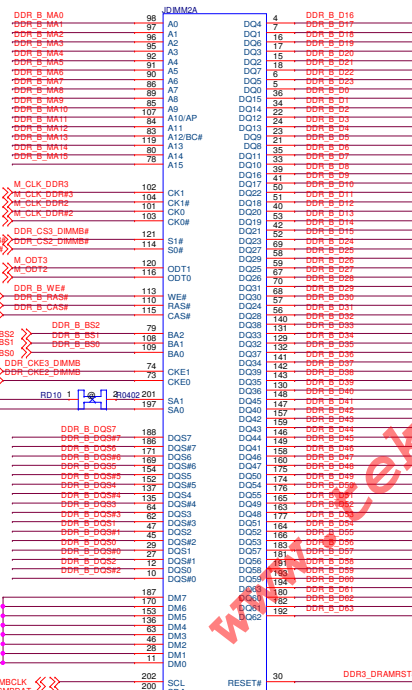
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



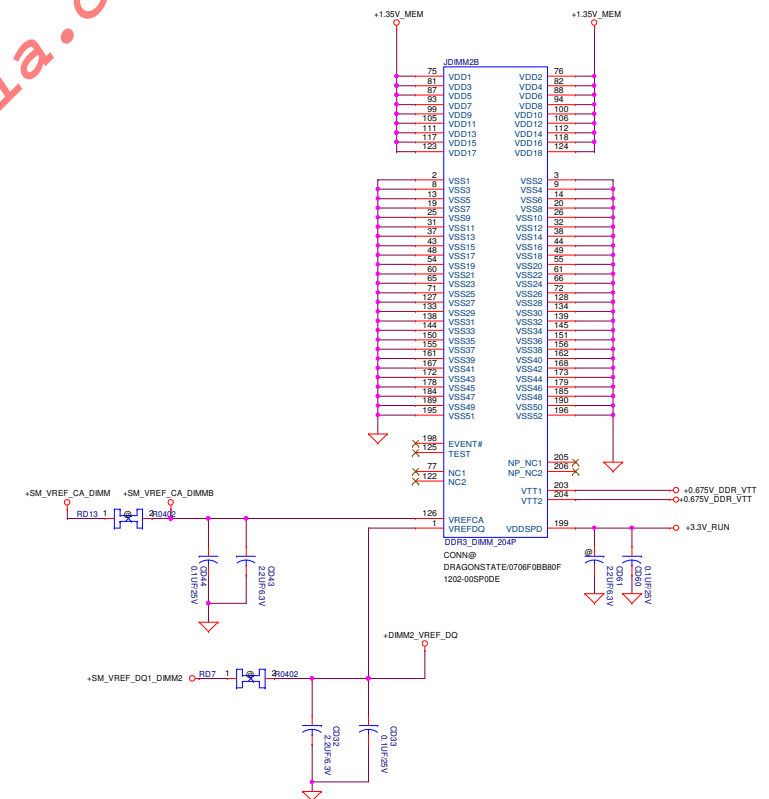
Layout Note:
Place near JDIMM1.203,204



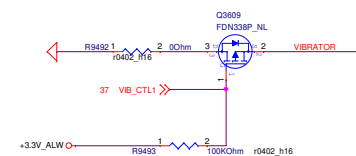
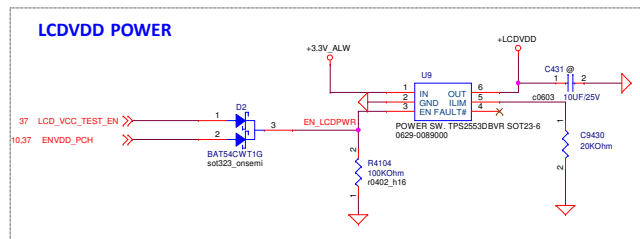
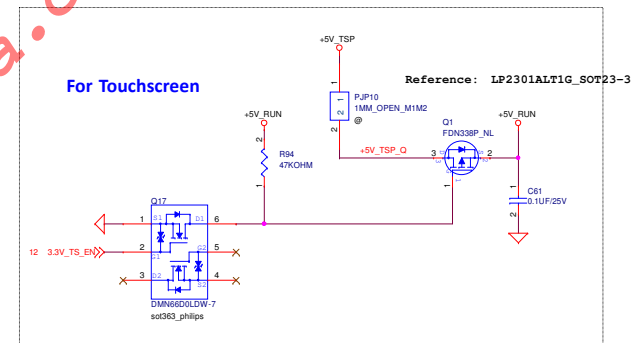
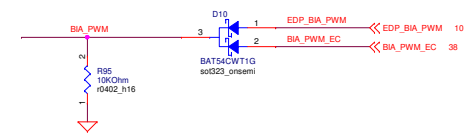
Interleaved Memory

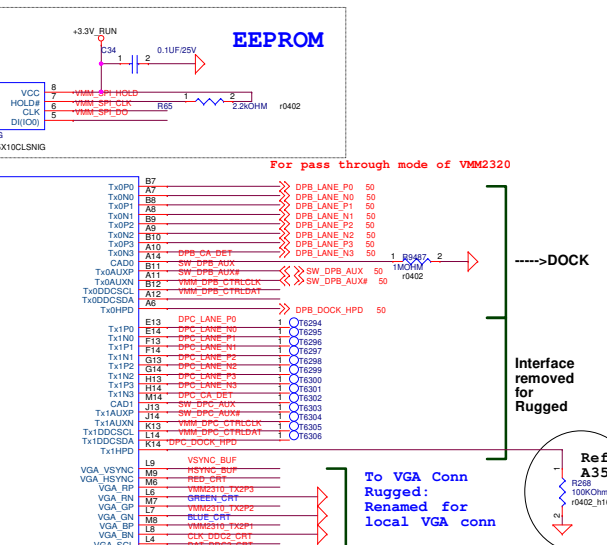
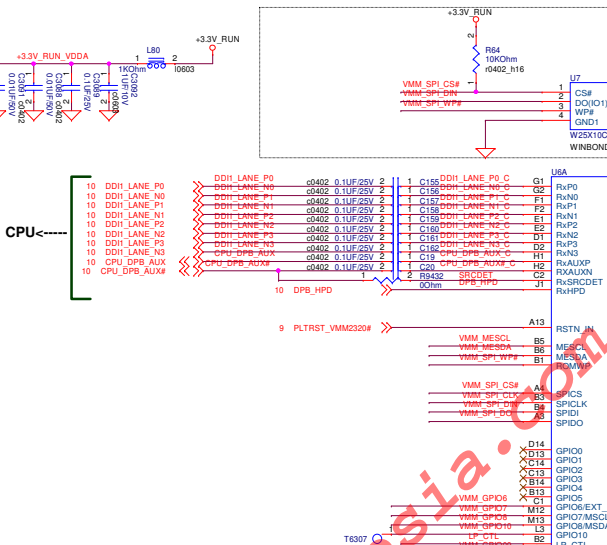
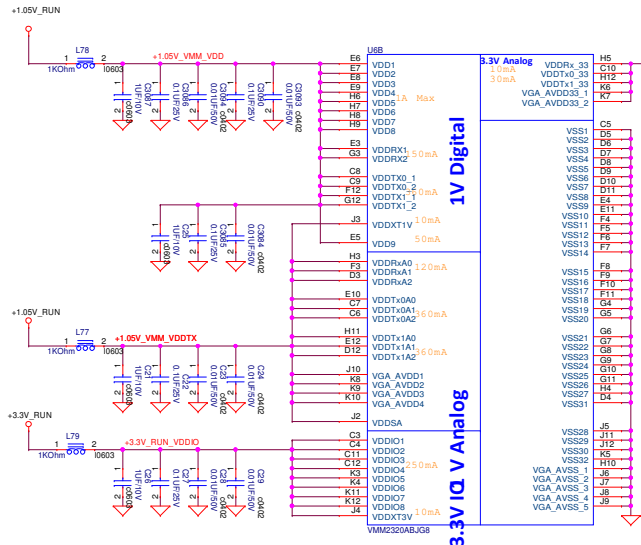


CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN



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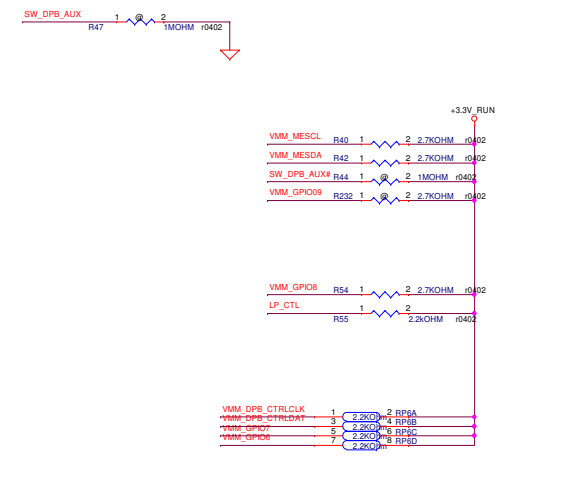
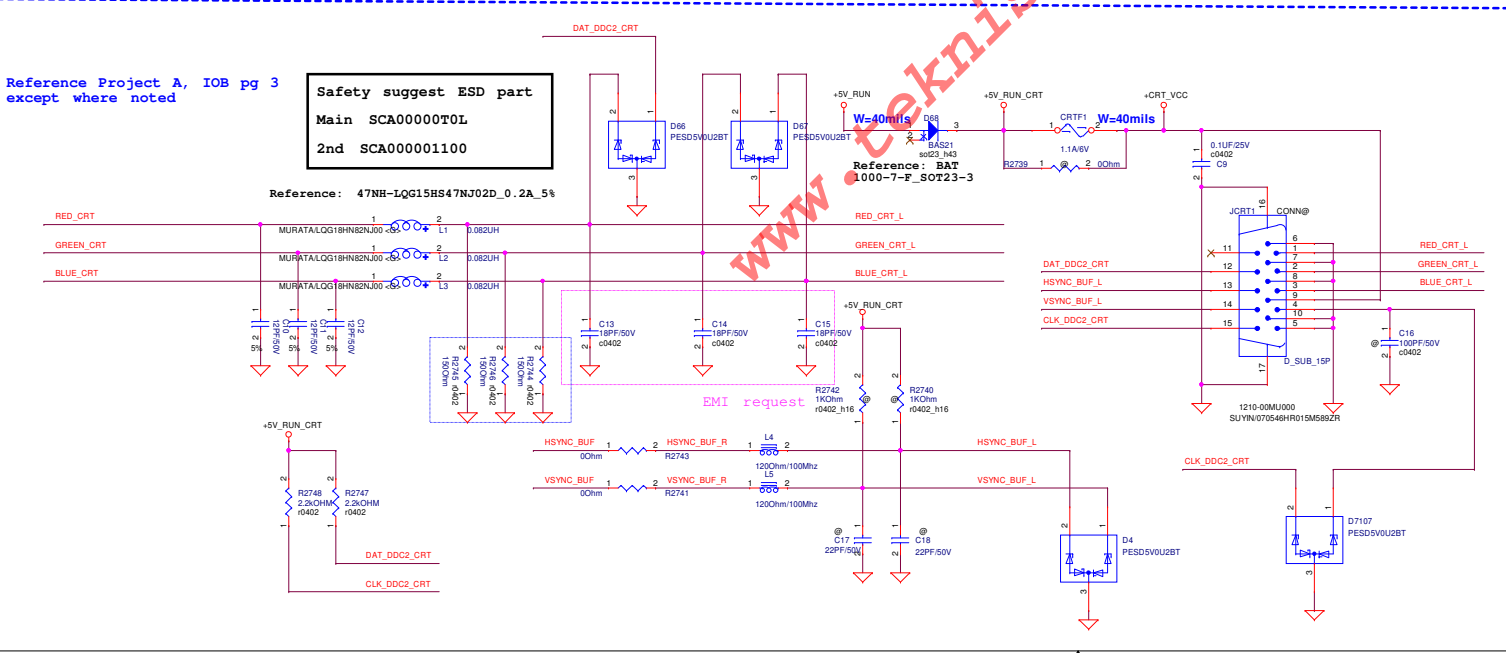


Reference Project A, pg 21
except where noted

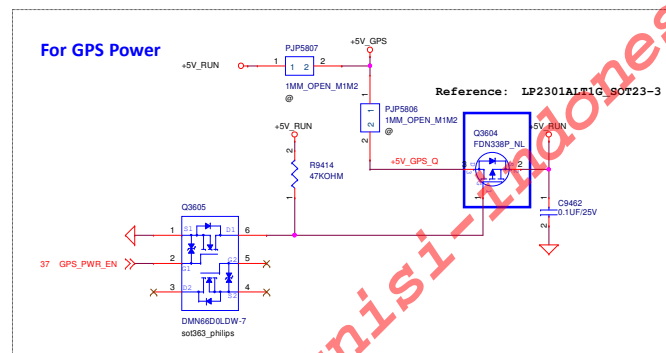
Reference Project A, IOB pg 3
except where noted

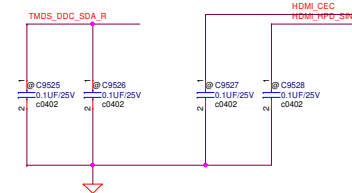
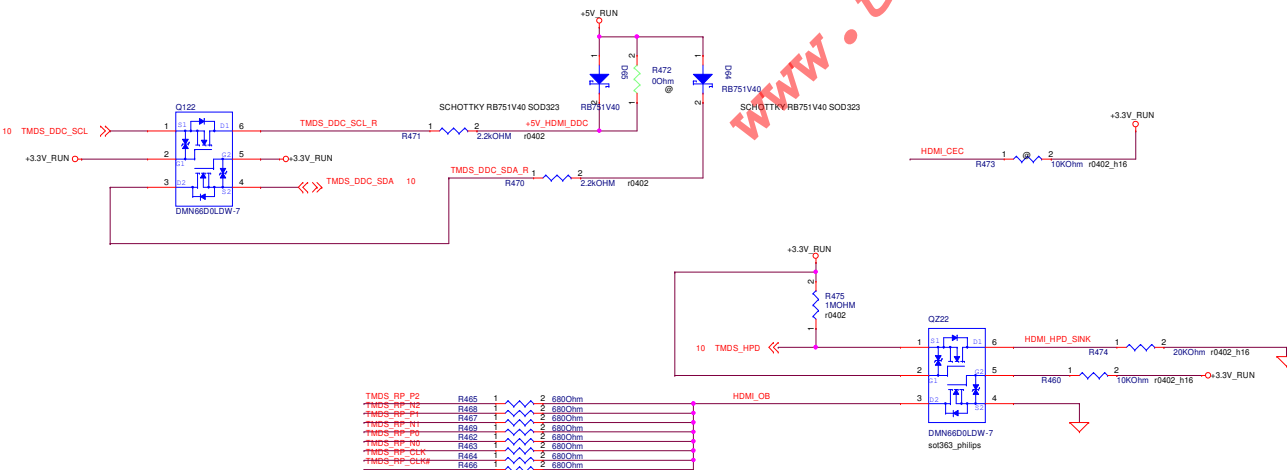
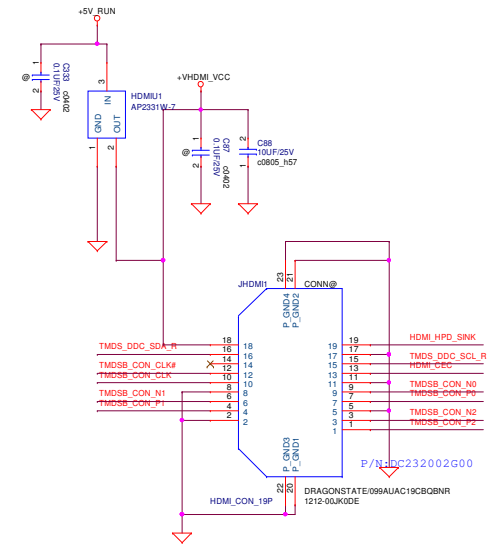
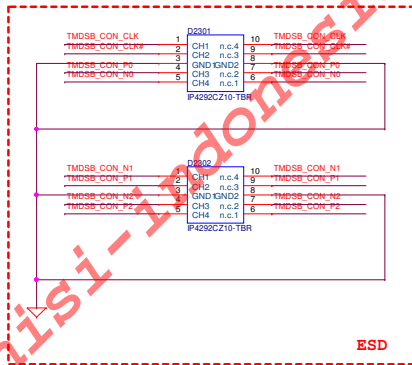
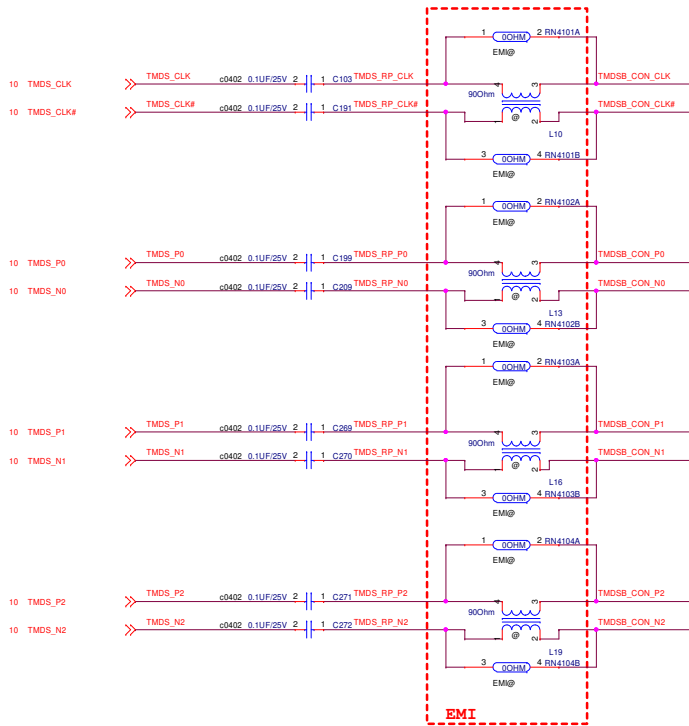
Safety suggest ESD part
Main SCA00000T0L
2nd SCA000001100

Reference: 47NH-LQG15HS47NJ02D_0.2A_5%



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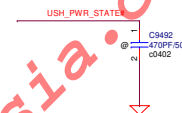
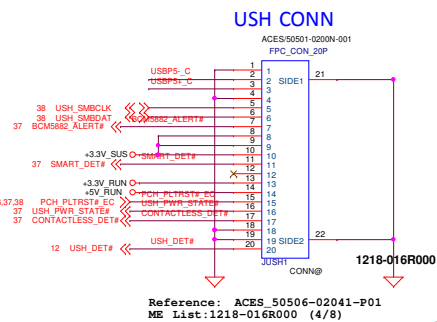
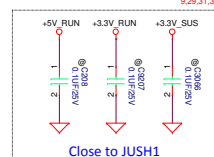




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DWG NO: CORE_B	DATE: Thursday, September 18, 2014	SHEET 23 of 65





SATA Re-Driver

Co-layout PS8520B/PS8527B

For PS8527B

Equalization level setting for Channel x (x=A/B)
internally tied to VDDQ2
[x_EQ2, x_EQ1] ==
U/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
U/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
N/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
N/L: for channel loss up to 11.3dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x (x=A/B)
internally tied to VDDQ2
[x_DE] ==
N: -3.5dB
L: 0dB
H: 1.5dB

For PS8520B

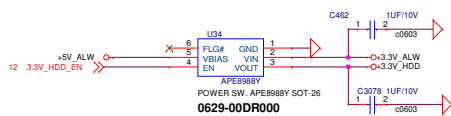
Pre-emphasis level setting for Channel A
3.3V tolerant. Internally pulled down at ~150K
[A_PRE1, A_PRE0] [A_EQ2, A_EQ1] in PS8527 ==
00: 0dB, no pre-emphasis
01: 1.5dB pre-emphasis is selected
10: 2.5dB pre-emphasis is selected
11: 3.5dB pre-emphasis is selected

Pre-emphasis level setting for Channel B
3.3V tolerant. Internally pulled down at ~150K
[B_PRE1, B_PRE0] [B_EQ2, B_EQ1] in PS8527 ==
00: 0dB, no pre-emphasis
01: 1.5dB pre-emphasis is selected
10: 2.5dB pre-emphasis is selected
11: 3.5dB pre-emphasis is selected

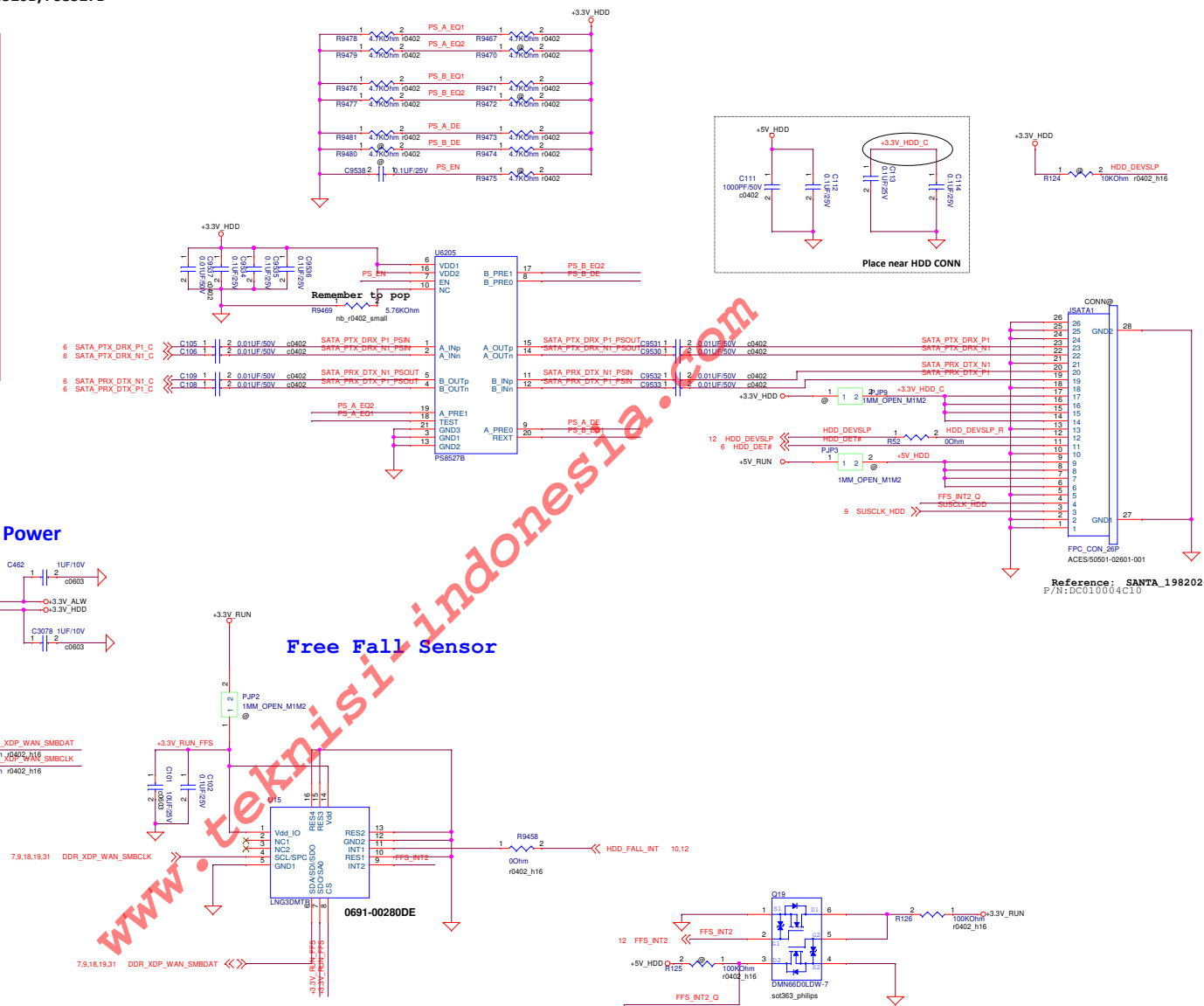
Chip test mode enable, internally pulled down
at ~150K
TEST[A_EQ1 in PS8527] ==
L: Normal operation
H: Test mode enable
For SATA/SAS PHY test, this pin should be pulled
to High

External resistor for output swing adjustment.
REXT[B_EQ1 in PS8527] need to be pulled down
with a 1% precision 4.99k ohm resistor, or left
open.

+3.3V Storage Power



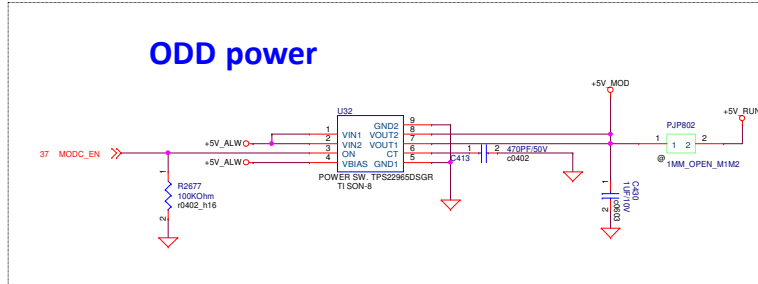
Free Fall Sensor



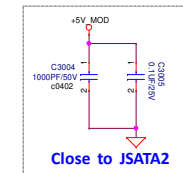
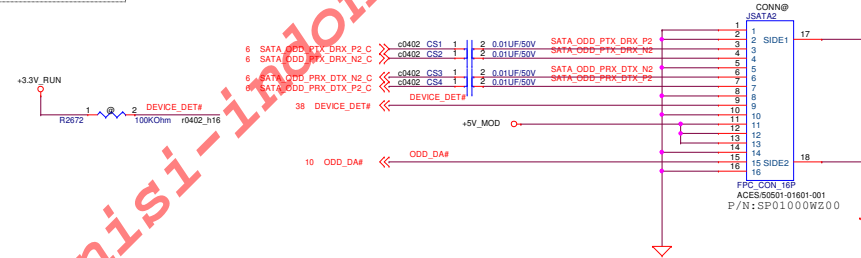
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	<p>DWG NO.: CORE_B</p>	<p>REV.: 2.2</p>	
	<p>DATE: Thursday, September 18, 2014</p>		
<p>SHEET: 25 of 65</p>			

ODD power



Reference: TYCO_1759838-1

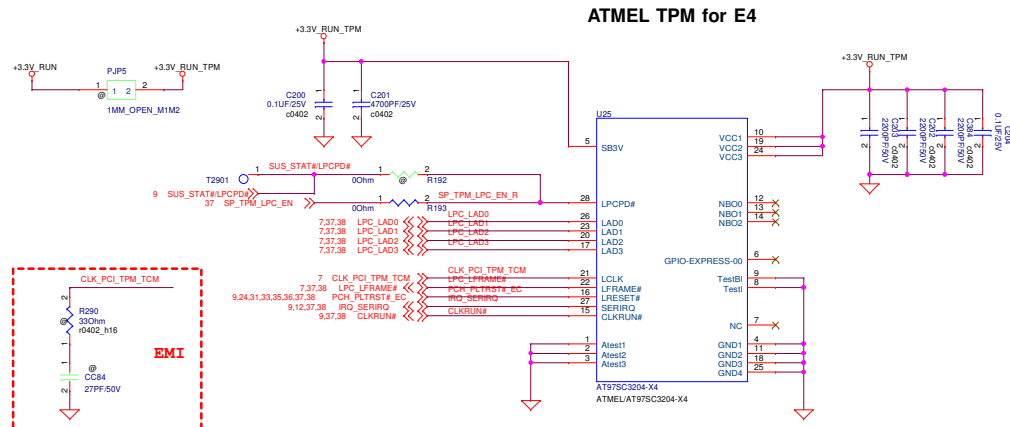


Close to JSATA2

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DWG NO. CORE_B	REV. 2.2	DATE Thursday, September 18, 2014 SHEET 26 of 65	



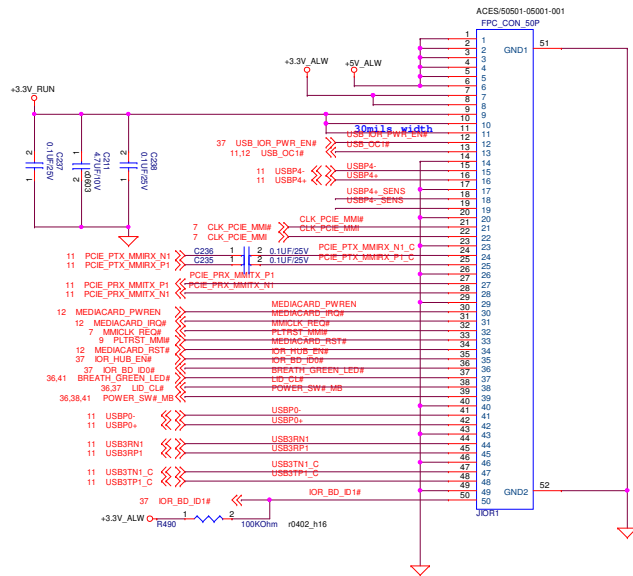


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DWG NO.	CORE_B	REV.	2.2
DATE	Thursday, September 18, 2014	SHEET	29 of 65



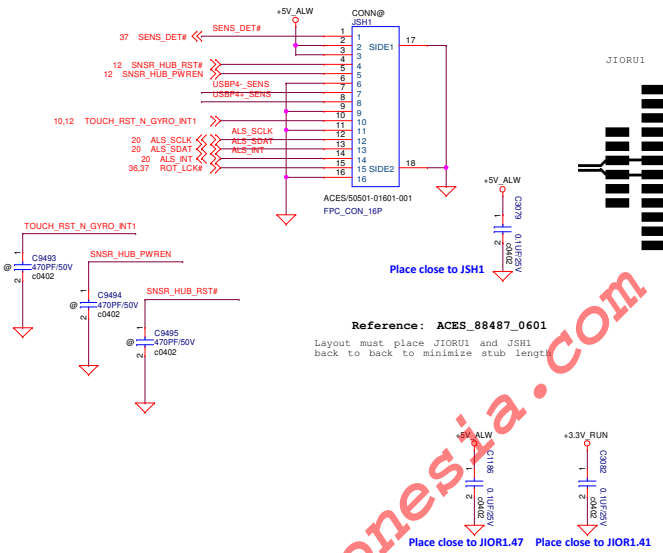
IOR USB+SD Connectors



Sensor HUB for Columbus.
JIORU1 USB2.0 unavailable when installed

New conn-6 pin,so delete below
signals which didn't appear in ARD.:

1. +5V_ALW
2. +3.3V_RUN
3. BREATH_LED#_Q
4. WIN_SW
5. D_TAB
6. D_CIM



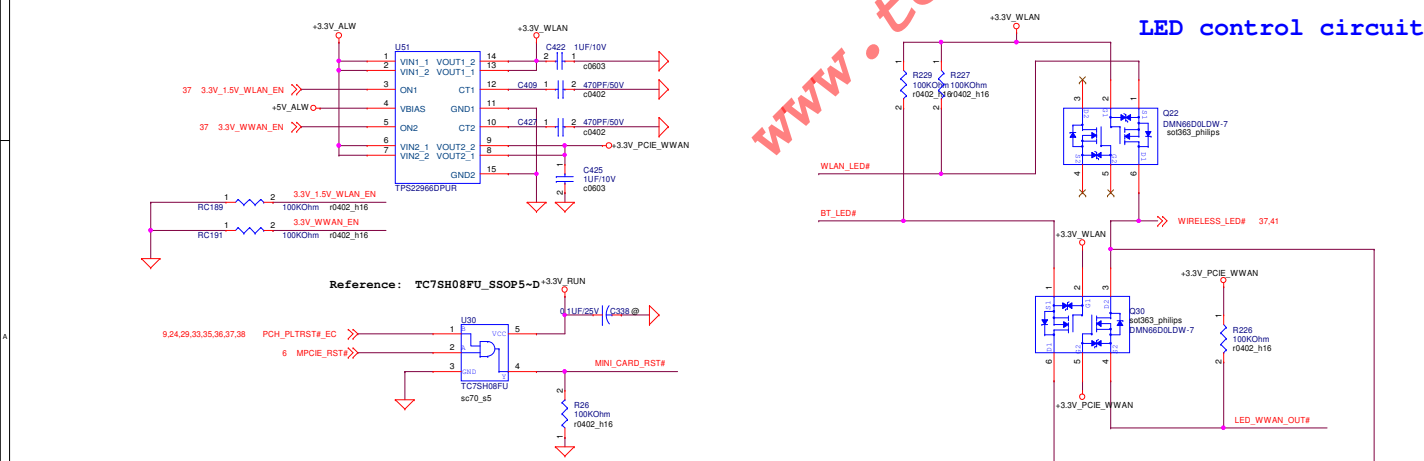
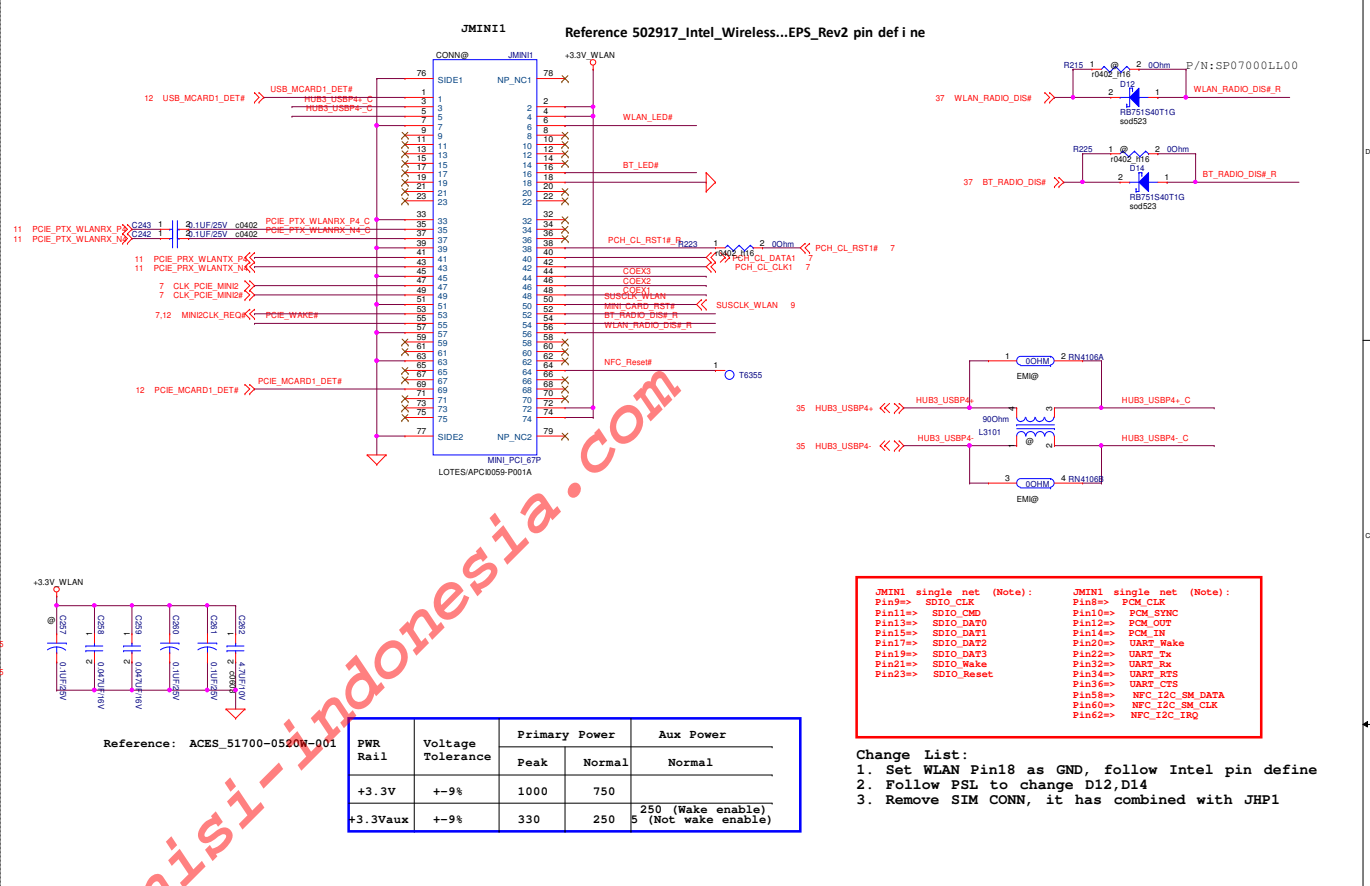
www.teknisi-indonesia.com

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PROPRIETARY NOTE		TITLE	
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SWD NO.	CORE_B	REV.	2.2
DATE	Thursday, September 18, 2014	SHEET	30 of 65



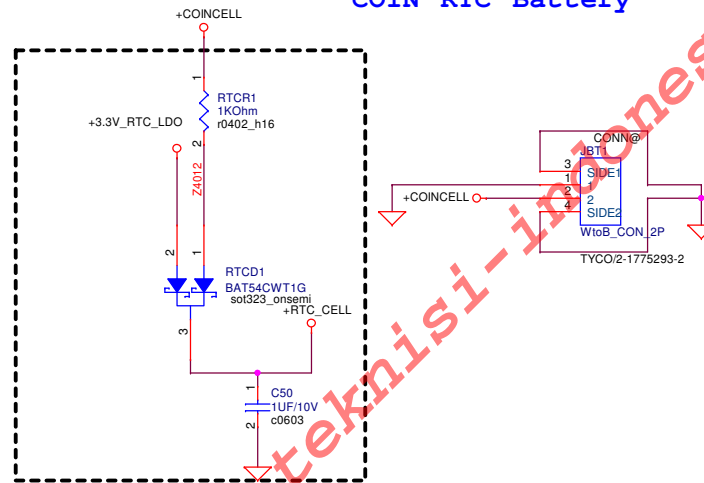
HMC: NGFF KEY-E WLAN/WiGi/BT H=8.5



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[illegible]

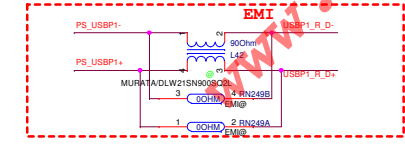
COIN RTC Battery

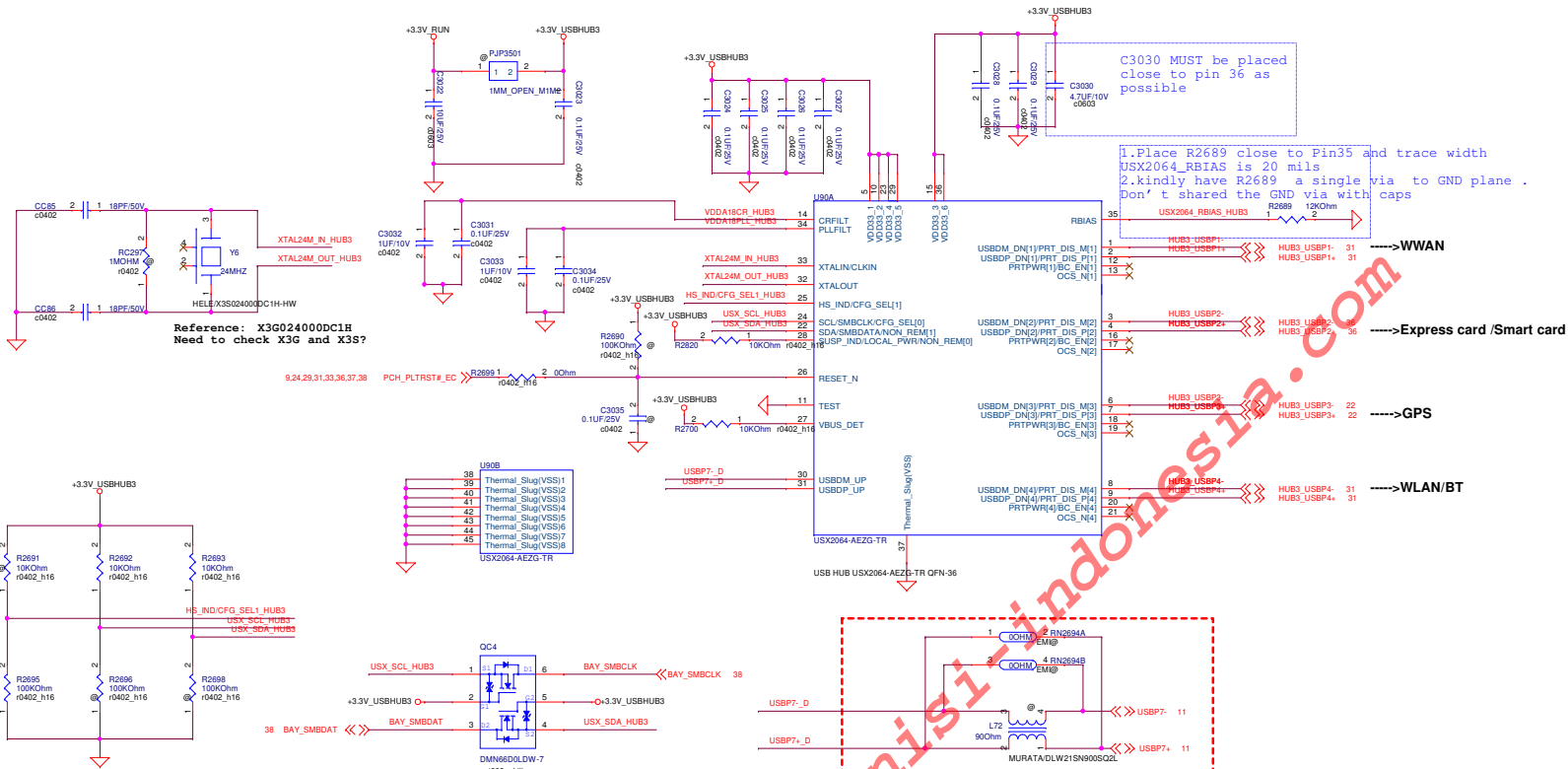


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DWG NO. CORE_B	REV. 2.2		
DATE Thursday, September 18, 2014	SHEET 32 of 65		

Config	SLG55594VTR	SLG55594AVTR
Pop	R9486, R9483	R288, R9484, Q3608
Depop	R288, R9484, Q3608	R9486, R9483





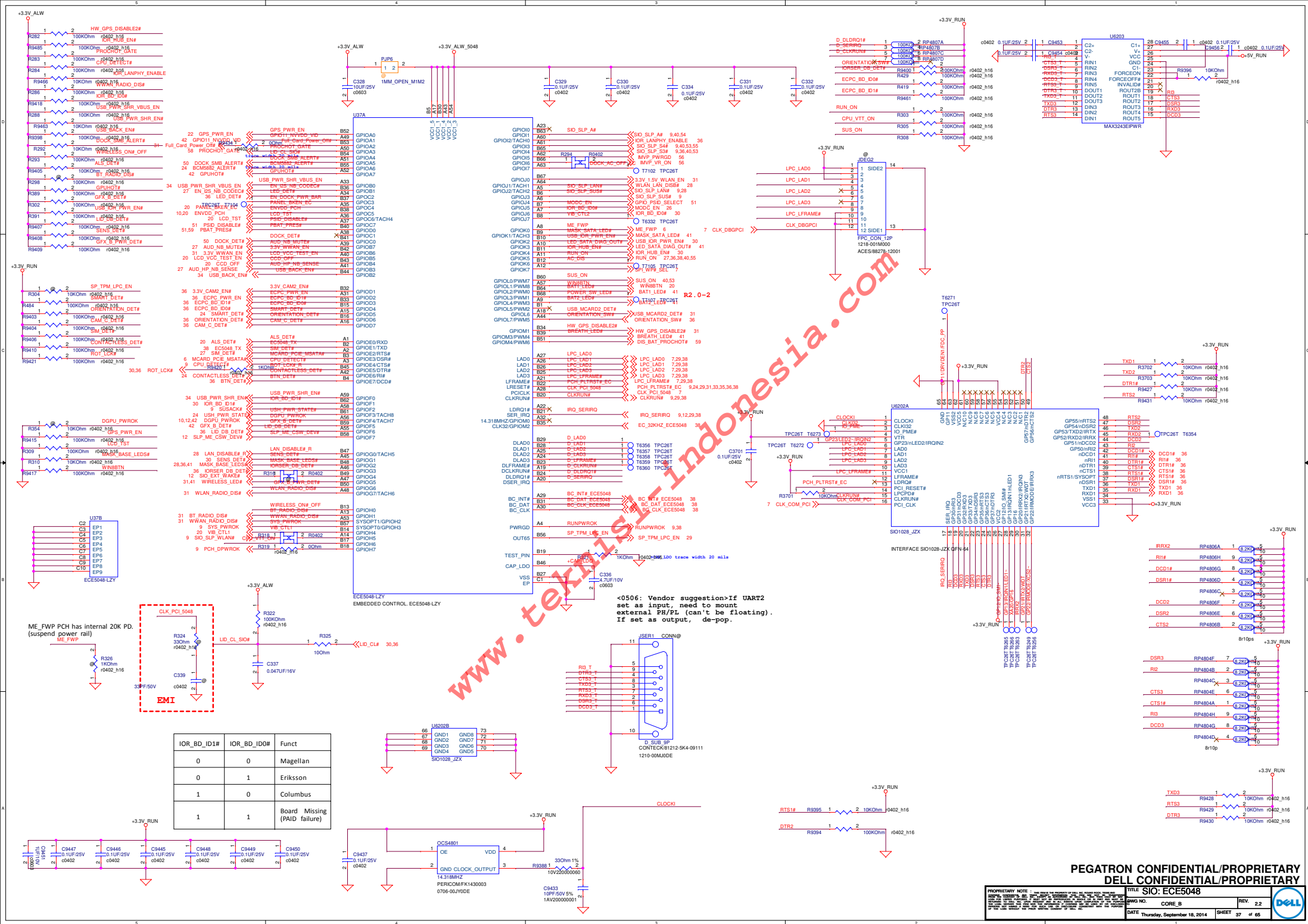
USX2064 CFG Selection Table

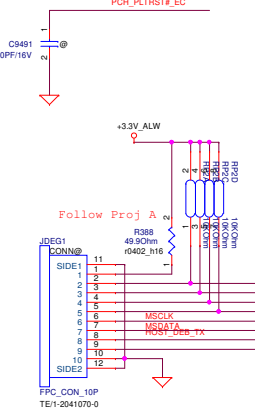
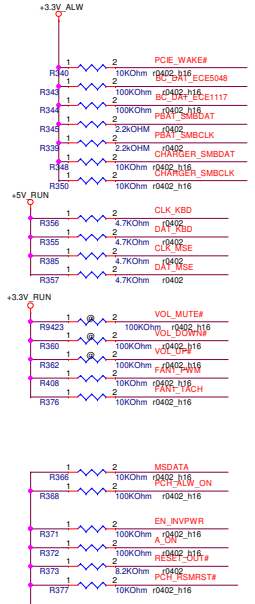
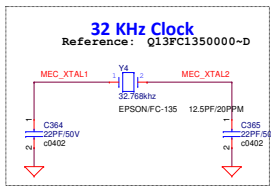
CFG_SEL[0]	0	1
CFG_SEL[1]	Default	SMBus slave device
0	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM

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	DWG NO.	CORE_B		
	DATE	Thursday, September 18, 2014	SHEET	35 of 65

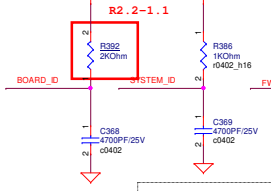
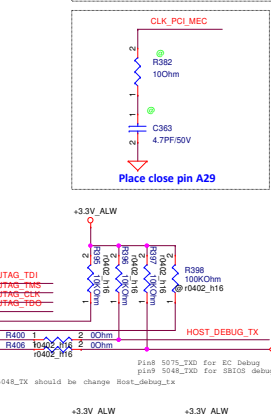
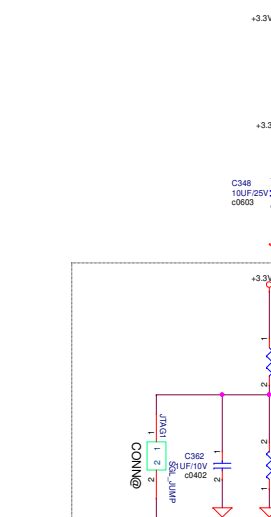




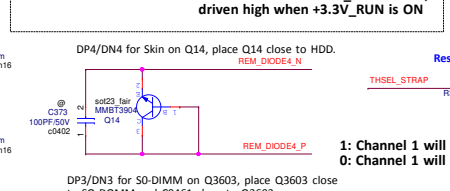
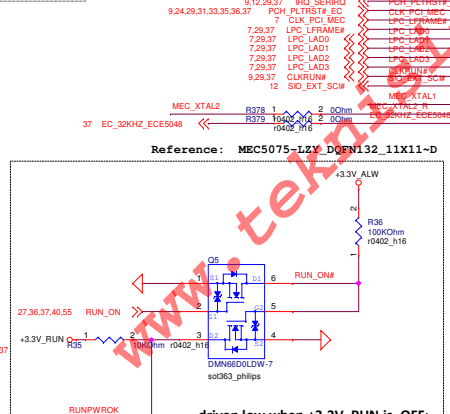
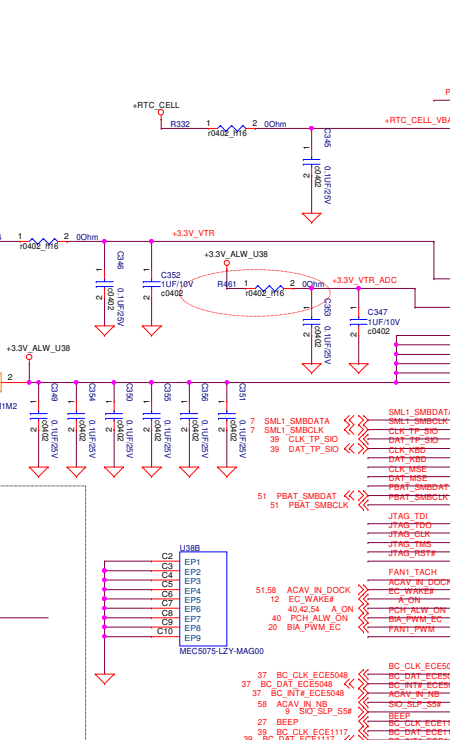


R392	C368	REV
240K 4700p	S00	
130K 4700p	S01	
62K 4700p	X01	
33K 4700p	X02	
8.2K 4700p	A00	
4.3K 4700p	A01	
2K 4700p	A02	
1K 4700p		

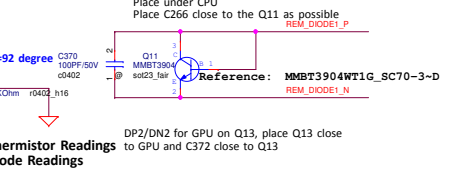
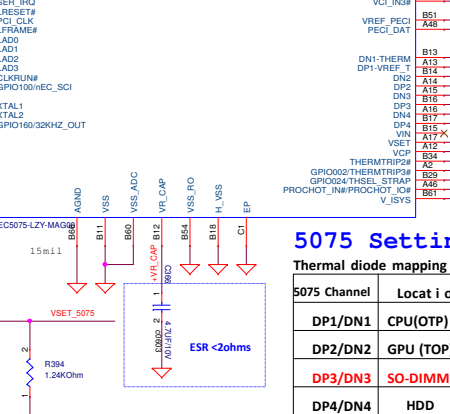
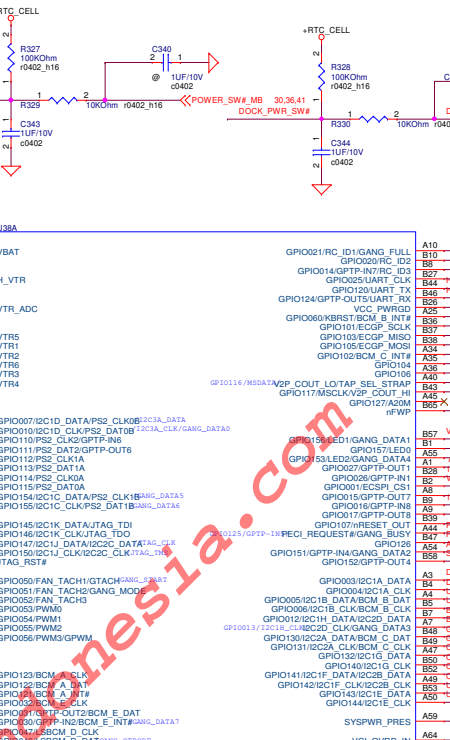
BOARD_ID rise time is measured from 5% to 68%



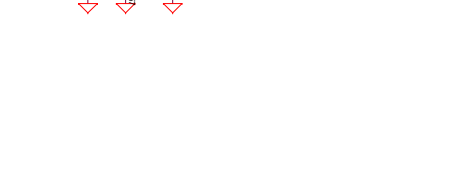
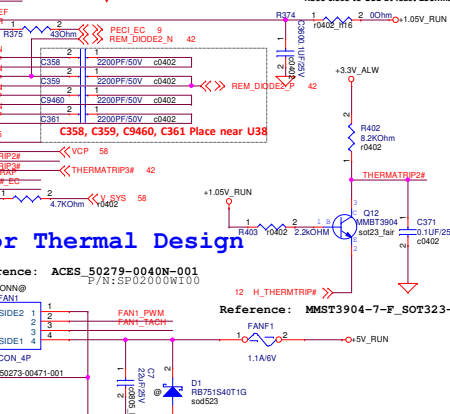
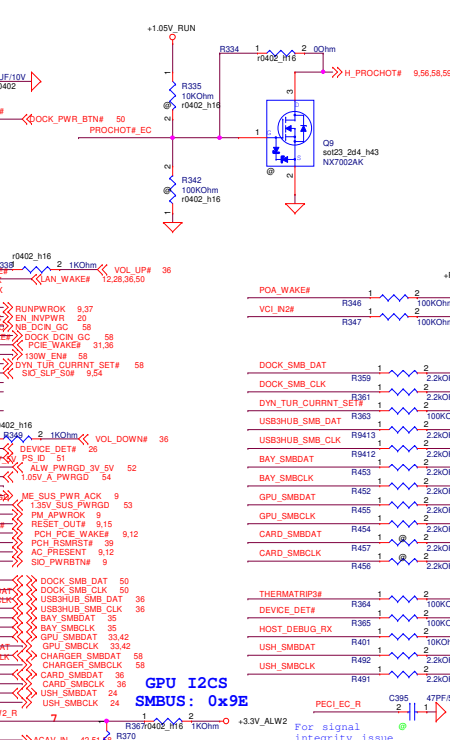
BOARD_ID rise time is measured from 5% to 68%



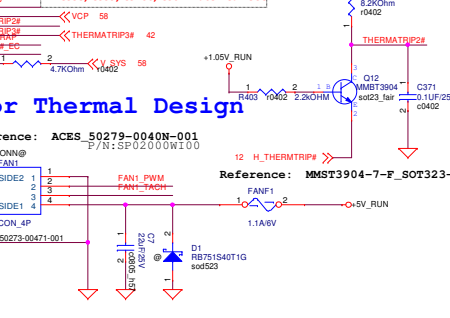
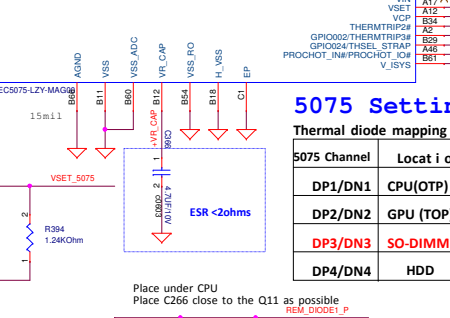
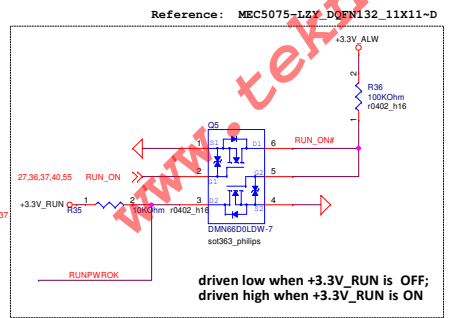
BOARD_ID rise time is measured from 5% to 68%



BOARD_ID rise time is measured from 5% to 68%

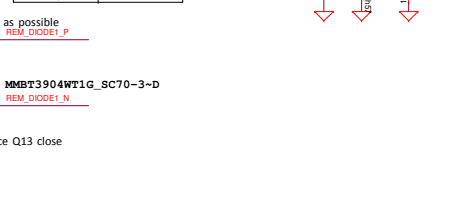


BOARD_ID rise time is measured from 5% to 68%

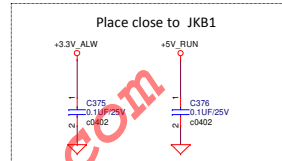
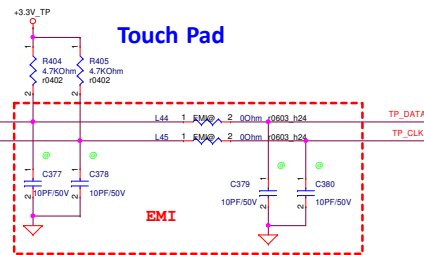
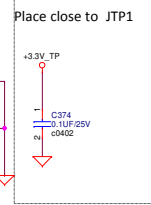
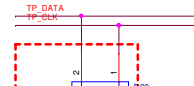


5075 Setting for Thermal Design

5075 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	GPU (TOP)
DP3/DN3	SO-DIMM
DP4/DN4	HDD



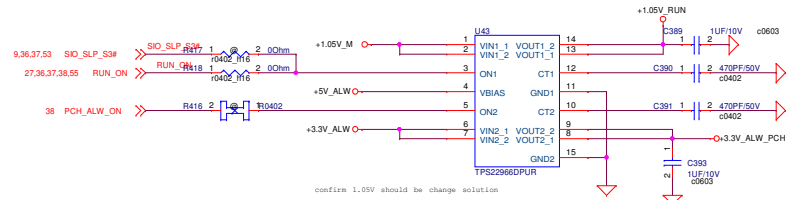
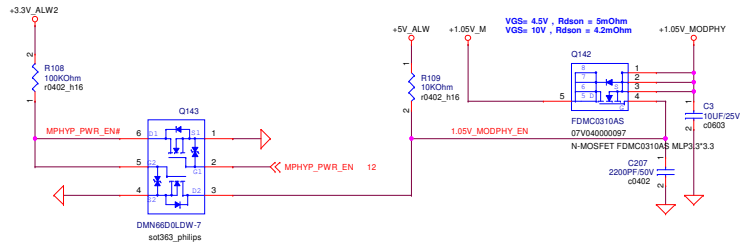
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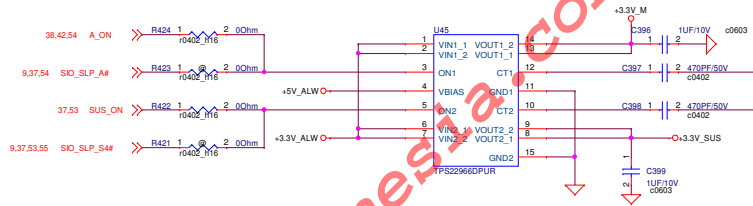
Reference: TC7SH08FU_SSP05-D

+3.3V_ALW_PCH/+1.05V_RUN source

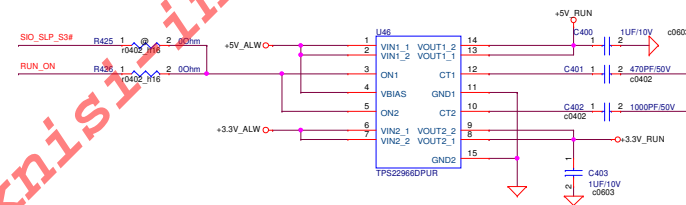
+1.05V_MODPHY source

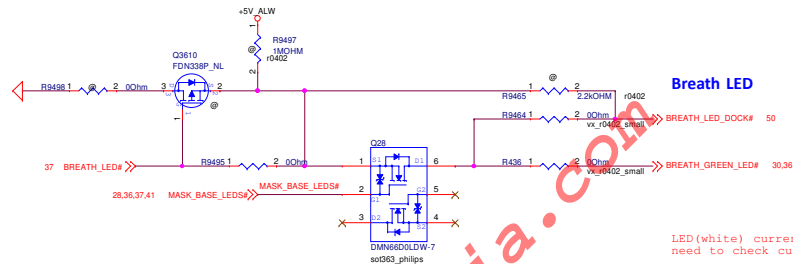
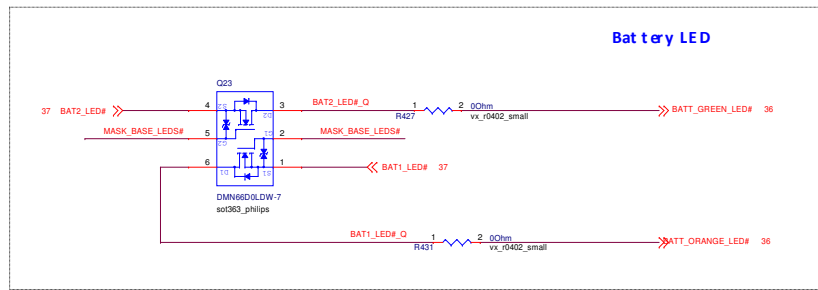
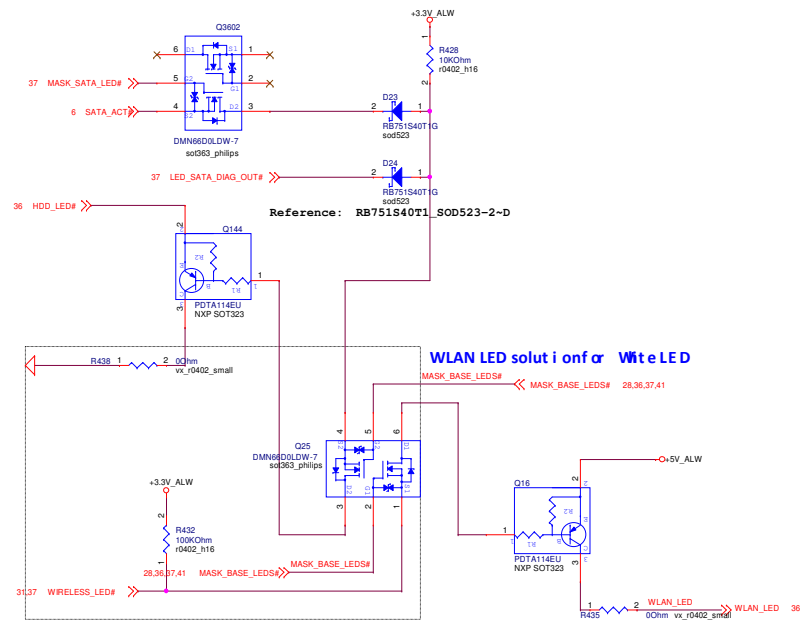


+3.3V_SUS/+3.3V_M source

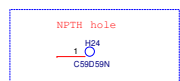
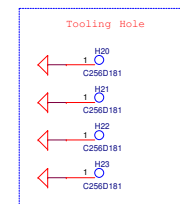
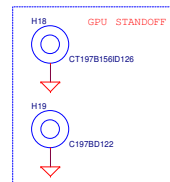
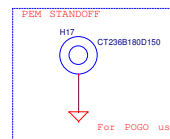
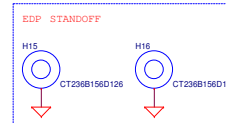
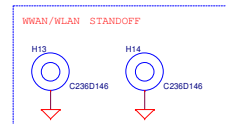
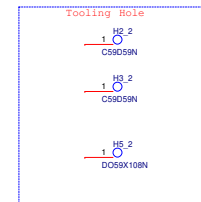
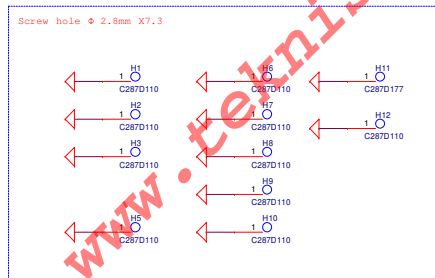
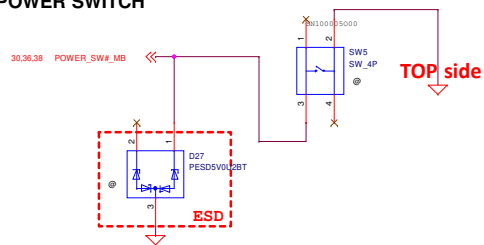


+3.3V_RUN/+5V_RUN source





POWER SWITCH

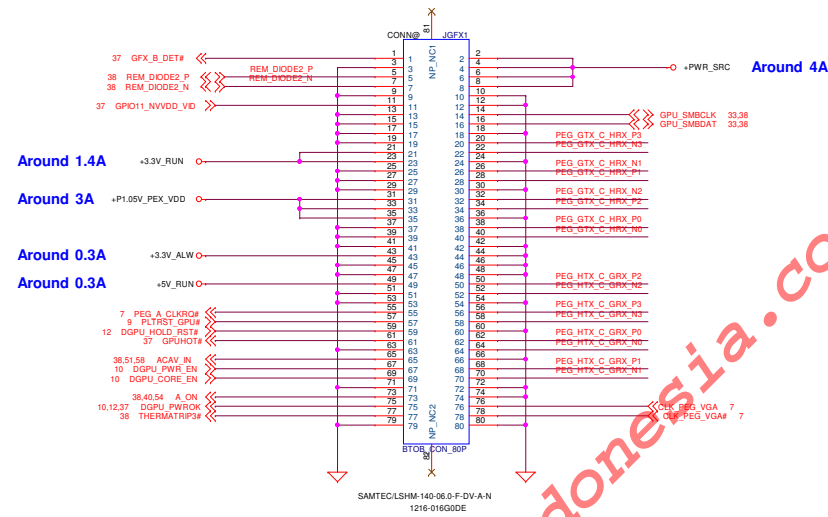


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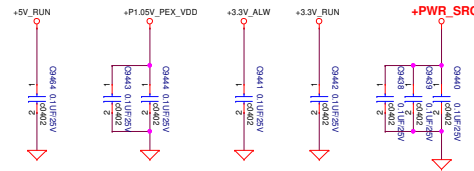
PROPRIETARY NOTE		TITLE	
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DWG NO.	CORE_B	REV.	2.2
DATE	Thursday, September 18, 2014	SHEET	41 of 65



11 PEG_HTX_C_GRX_P[0..3] << PEG_HTX_C_GRX_P[0..3]
 11 PEG_HTX_C_GRX_N[0..3] << PEG_HTX_C_GRX_N[0..3]
 11 PEG_GTX_C_HRX_P[0..3] << PEG_GTX_C_HRX_P[0..3]
 11 PEG_GTX_C_HRX_N[0..3] << PEG_GTX_C_HRX_N[0..3]



For GFX conn power:
 1. +PWR_SRC : 3.3A
 2. +P1.05V_PEX_VDD : 1.15A
 3. +3.3V_RUN : 0.342A
 4. +3.3V_ALW : 0.04A




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<small>DWG NO.</small> CORE_B		<small>REV.</small> 2.2		
<small>DATE</small> Thursday, September 18, 2014		<small>SHEET</small> 44 of 65		

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DWG NO. CORE_B		REV. 2.2		
DATE Thursday, September 18, 2014		SHEET 45 of 65		

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	DWG NO. CORE_B	REV. 2.2	
	DATE Thursday, September 18, 2014	SHEET 46 of 65	

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	DWG NO. CORE_B	REV. 2.2	
	DATE Thursday, September 18, 2014	SHEET 47 of 65	

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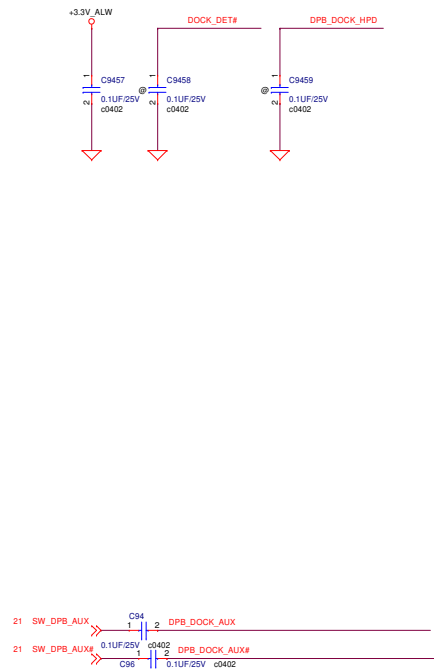
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	DWG NO. CORE_B	REV. 2.2	
	DATE Thursday, September 18, 2014	SHEET 48 of 65	

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DWG NO. CORE_B		REV. 2.2		
DATE Thursday, September 18, 2014		SHEET 49 of 65		



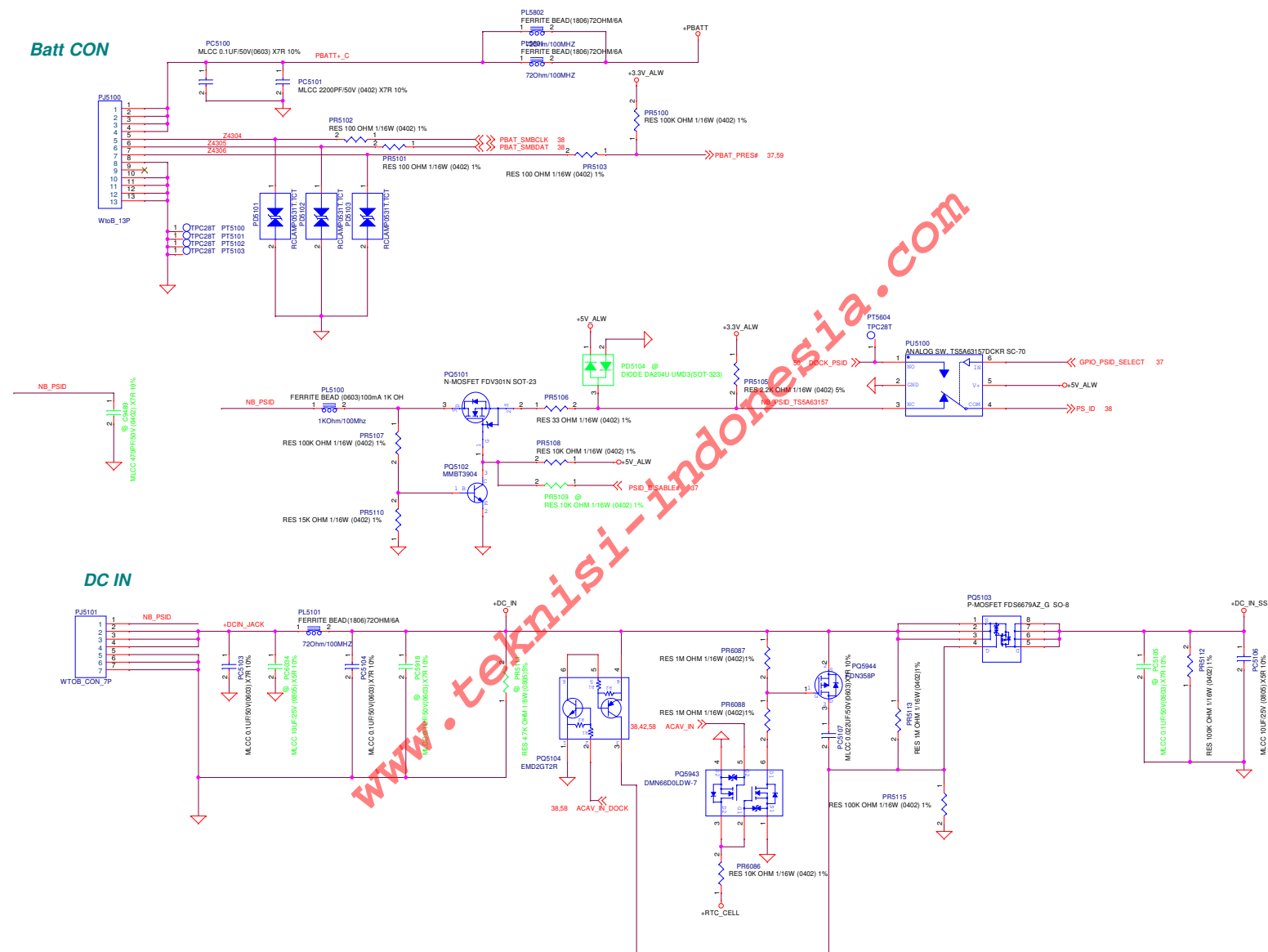
DP1.2
 4-Lane
 from
 Video SW

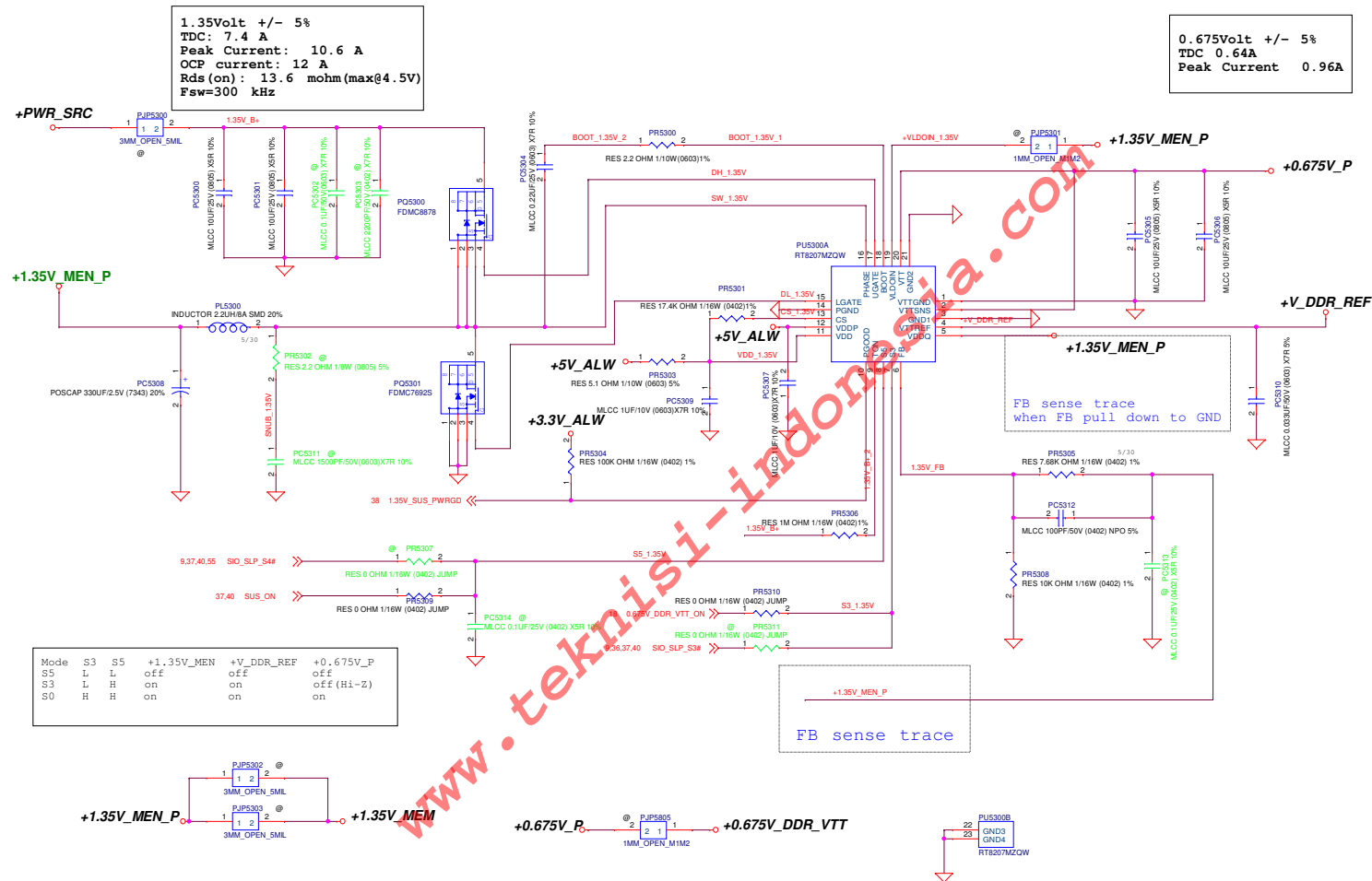
USB3.0



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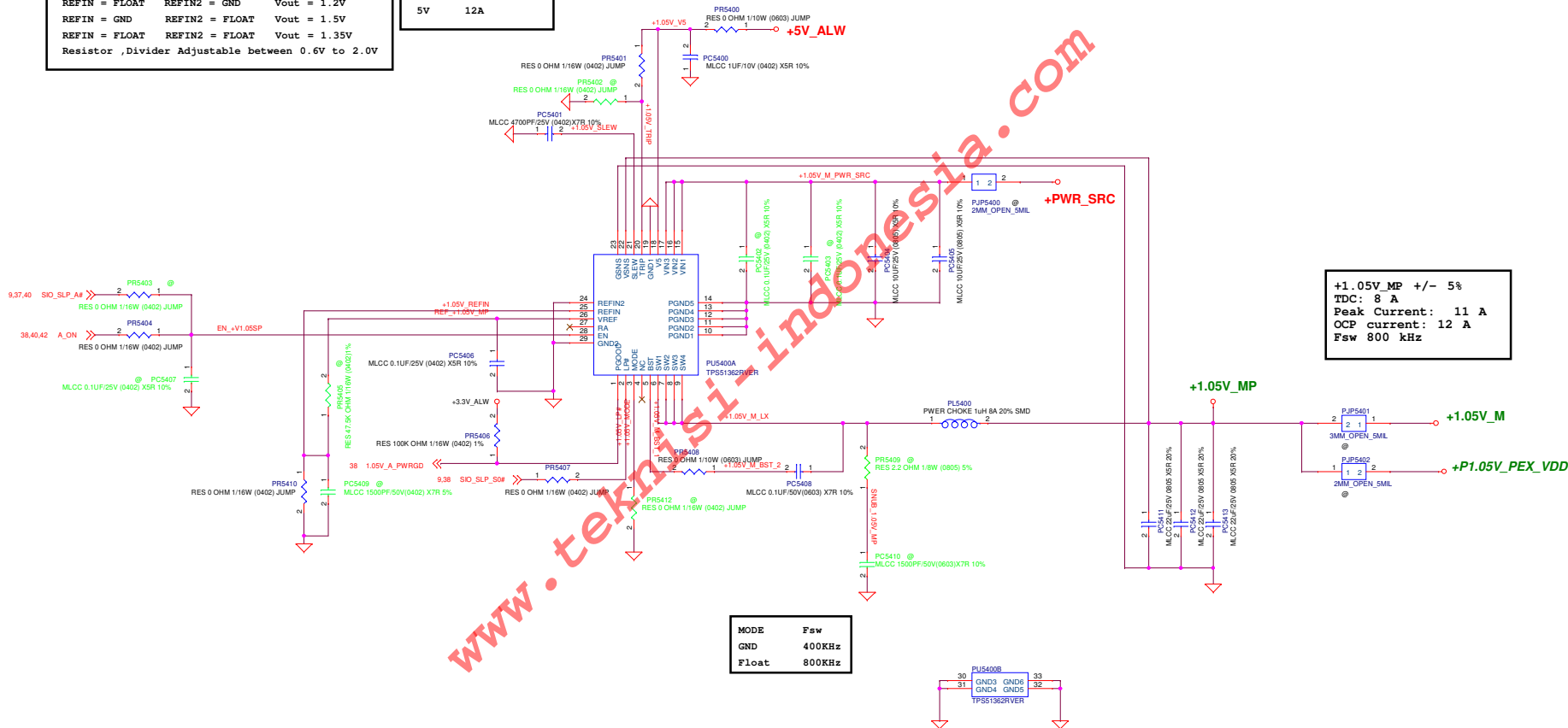
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	REV. 2.2	REV. 2.2
DATE Thursday, September 18, 2014	SHEET 53 of 65	



REFIN Table			
REFIN = GND	REFIN2 = GND	Vout = 1.05V	
REFIN = FLOAT	REFIN2 = GND	Vout = 1.2V	
REFIN = GND	REFIN2 = FLOAT	Vout = 1.5V	
REFIN = FLOAT	REFIN2 = FLOAT	Vout = 1.35V	
Resistor ,Divider Adjustable between 0.6V to 2.0V			

TRIP	OC Limit (A)
GND	8A
5V	12A



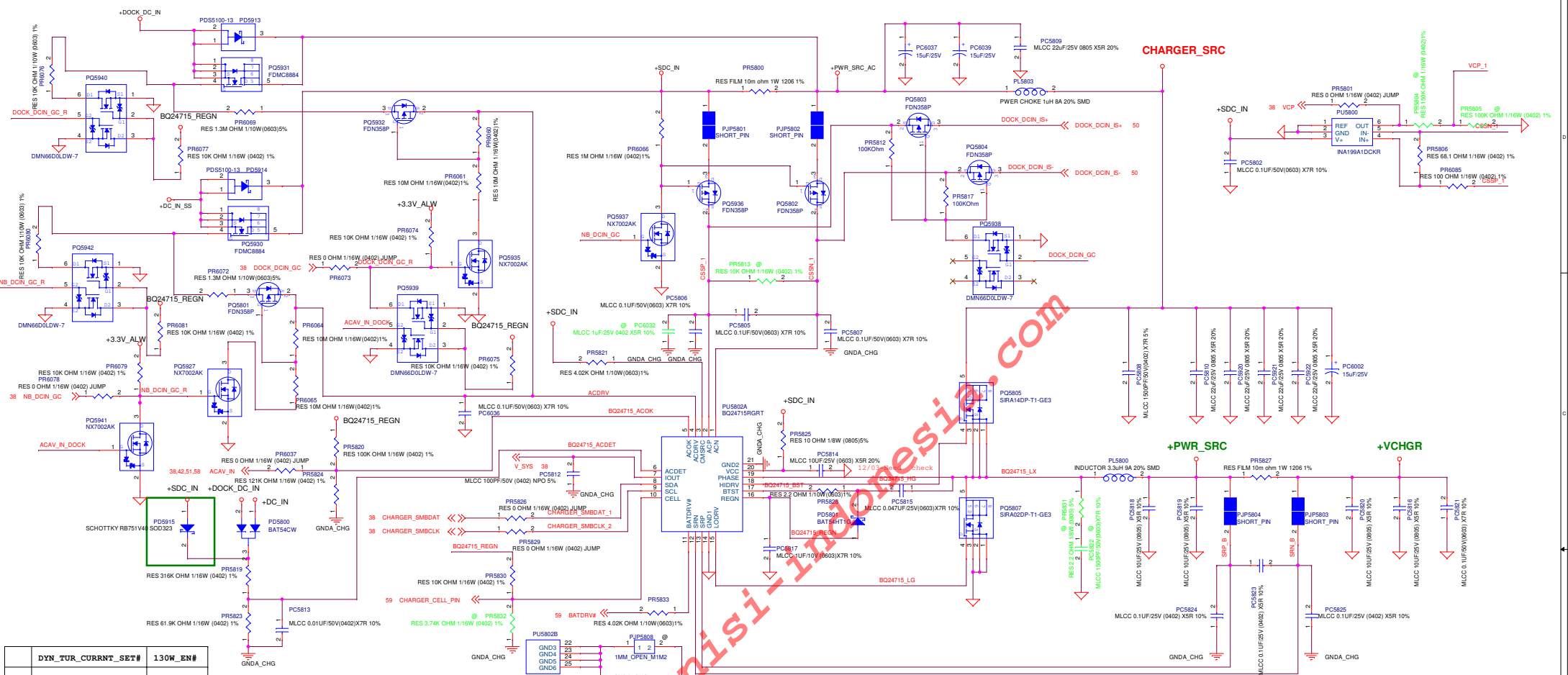
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DATE: Thursday, September 18, 2014	SHEET: 54 of 65	REV: 2.2	



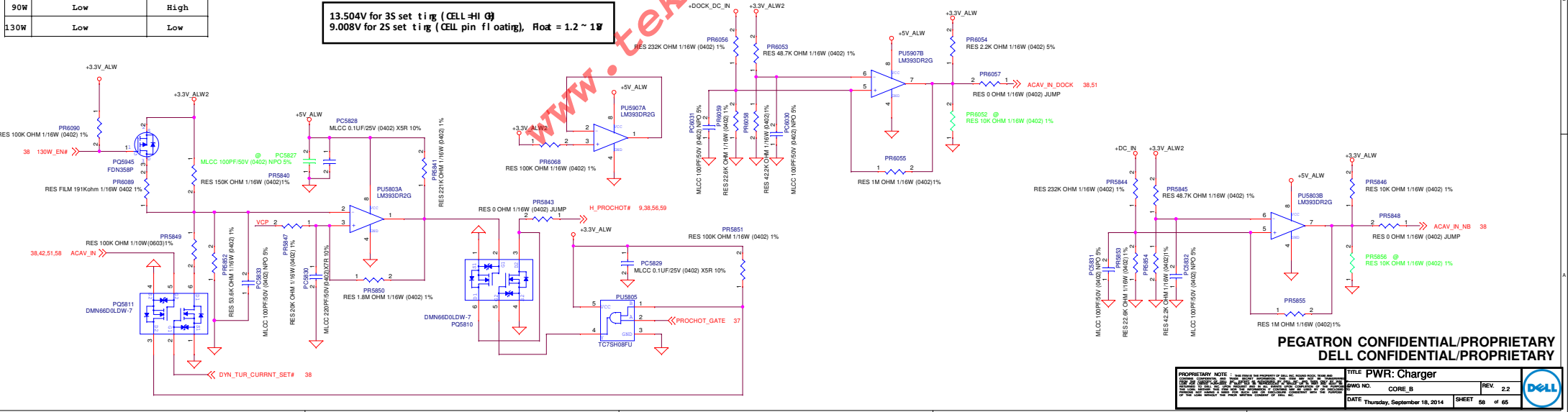
The diagram shows a PCB layout for the +VCC_CORE power plane. It features a 4x5 grid of decoupling capacitors. The top rail is connected to +VCC_CORE, and the bottom rail is connected to GND. The capacitors are arranged in four rows and five columns. Each capacitor is labeled with its value: 22µF/25V 0805 X5R 20%.

Row	Col 1	Col 2	Col 3	Col 4	Col 5
1	PC5700	PC5701	PC5702	PC5703	PC5704
2	PC5705	PC5706	PC5707	PC5708	PC5709
3	PC5710	PC5711	PC5712	PC5713	PC5714
4	PC5715	PC5716	PC5717	PC5718	PC5719
5	PC5720	PC5721	PC5722	PC5723	PC5724
6	PC5725	PC5726	PC5727	PC5728	PC5729



	DYN_TUR_CURRNT_SET#	130W_EN#
65W	High	High
90W	Low	High
130W	Low	Low

13.504V for 3S set ting (CELL+H G)
9.008V for 2S set ting (CELL pin fl oating), Roat = 1.2 ~ 1W



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<small>DWG NO.</small>	CORE_B	<small>REV.</small>	2.2
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<small>DWG NO.</small>	CORE_B	<small>REV.</small>	2.2	
<small>DATE</small>	Thursday, September 18, 2014	<small>SHEET</small>	61 of 65	

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DWG NO. CORE_B		REV. 2.2		
DATE Thursday, September 18, 2014		SHEET 62 of 65		

Page		Date	Page Owner	Source	Page Heritage List Modifications	Page 1	PIR items applied
P01-Cover Page		01/04/12		Alpine	Changed for Fleet Project		
P02-Block Diagram - main		01/04/12		Alpine	Leveraged, 50% different		F2, F3
P03-Index and Configuration		01/04/12		Alpine	Leveraged, 50% different		
P04-UMA Power Rail		01/04/12		Alpine	Leveraged, 50% different		
P05-SMBus block diagram-UMA		01/04/12		Alpine	Leveraged, 50% different		
P06-MCP (1/12) RTC, SATA, HAD, JTAG		01/04/12		Alpine	No changes from Alpine		A31
P07-MCP (2/12) CLK, SMB, SPI, LPC, CL		01/04/12		Alpine	SMBus reallocation		
P08-MCP (3/12) DDR3		01/04/12		Alpine	No changes from Alpine		
P09-MCP (4/12) PM, JTAG, MISC		01/04/12		Alpine	No changes from Alpine		
P10-MCP (5/12) DDI, EDP, GPIO		01/04/12		Alpine	DPB directly to VGA chip		A6, A17
P11-MCP (6/12) PCIE, USB		01/04/12		Alpine	Remapped		
P12-MCP (7/12) GPIO, LPIO, MISC		01/04/12		Alpine	No changes from Alpine		A10, A23
P13-MCP (8/12) CFG, RSVD		01/04/12		Alpine	No changes from Alpine		
P14-MCP (9/12) TP, RSVD		01/04/12		Alpine	No changes from Alpine		
P15-MCP (10/12) Power		01/04/12		Alpine	No changes from Alpine		A15
P16-MCP (11/12) Power		01/04/12		Alpine	No changes from Alpine		A14
P17-MCP (12/12) VSS		01/04/12		Alpine	No changes from Alpine		
P18-DDRIII DIMM1		01/04/12		Alpine	No changes from Alpine		A8
P19-DDRIII DIMM2		01/04/12		Alpine	No changes from Alpine		A8
P20-eDP & Touch Screen		01/04/12		Alpine	No LVDS		A5
P21-IDT VMM2310 DPtoVGA & Conn		01/04/12		Alpine	No MST huub		A11, A12
P22-GPS Conn		01/04/12		E3			
P23-HDMI Conn		01/04/12		Alpine	No changes from Alpine		A24
P24-Security Conn		01/04/12		Goliad	No MSI huub Power control signal		
P25-HDD Conn		01/04/12		Alpine	Connector changed		A18
P26-ODD module		01/04/12		Alpine	Connector changed		
P27-Azalia (HD) Codec - ALC3226		01/04/12		Alpine	Remove second mic/dock audio		A20, A21, A27
P28-LAN Lewisville / LAN SW		01/04/12		Alpine	Remove LAN switch		A10, A13
P29-TPM/FP		01/04/12		Alpine	Remove FPR		
P30-IOR PCIE Conn		01/04/12		Fleet	New		
P31-Mini Card/SIM Card		01/04/12		Alpine	mSATA and PCIE?		A13

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DATE Thursday, September 18, 2014		SHEET 63 of 65						

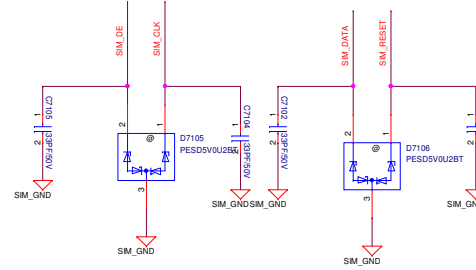
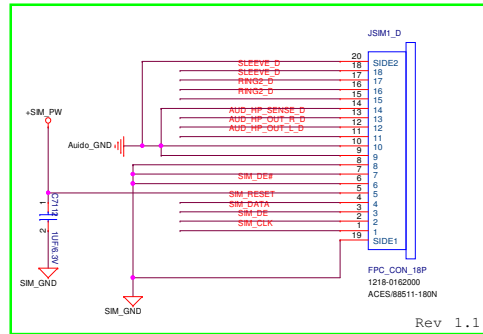
Page	Date	Page Owner	Source	Page Heritage List Modifications	Page 2	PIR items applied
P32-RTC Battery	01/04/12		Alpine	No changes from Alpine		
P33-USB2.0 HUB2-USX2064	01/04/12		Alpine	Changed for Fleet port map		
P34-USB on MB/Redriver	01/04/12		Alpine	No changes from Alpine		F3
P35-USB2.0 HUB3-USX2064	01/04/12		Alpine	New for Fleet		
P36-I/O Conn	01/04/12		Alpine	IOR connector replaces IOB, JSH1 added		A3, F2
P37-SIO & GPIO ECE5048	01/04/12		Alpine	Removed dock and used UART GPIOs		A9, A22, A25
P38-KBC & GPIO MEC5075	01/04/12		Alpine	No changes from Alpine		A16
P39-KB/TP/RSMRST	01/04/12		Alpine	No changes from Alpine		A18
P40-Power control	01/04/12		Alpine	No changes from Alpine		A11, A12, A26
P41-PAD & ME & LED	01/04/12		Alpine	No changes from Alpine		
P42-NV(1/5)-PCIE	01/04/12		Alpine	No changes from Alpine		A13
P43-NV(2/5)-IFP_ABCDEF_DAC_XTAL	01/04/12		Alpine	No changes from Alpine		
P44-NV(3/5)-POWER_GND	01/04/12		Alpine	No changes from Alpine		
P45-NV(4/5)-GPIO_BIOS_STRAP	01/04/12		Alpine	No changes from Alpine		A19
P46-NV(5/5)-MEMORY_FBA	01/04/12		Alpine	No changes from Alpine		
P47-VRAM_DDR3_A Lower	01/04/12		Alpine	No changes from Alpine		
P48-VRAM_DDR3_A Upper	01/04/12		Alpine	No changes from Alpine		
P49-VGA_DC/DC Interface	01/04/12		Alpine	No changes from Alpine		
P50-Blank	01/04/12		Alpine			
P51-PWR_DCIIN	01/04/12		Alpine	No changes from Alpine		
P52-PWR_+5V/+3.3V	01/04/12		Alpine	No changes from Alpine		
P53-PWR_+1.35V_MEM/+0.675V_DDR	01/04/12		Alpine	No changes from Alpine		
P54-PWR_+1.05VITTP	01/04/12		Alpine	No changes from Alpine		
P55-PWR_1.5V_RUN	01/04/12		Alpine	No changes from Alpine		
P56-PWR_VCORE	01/04/12		Alpine	No changes from Alpine		
P57-PWR_PROCESSOR DECOUPLING	01/04/12		Alpine	No changes from Alpine		
P58-PWR_Charger	01/04/12		Alpine	No changes from Alpine		
P59-PWR_Selector	01/04/12		Alpine	No changes from Alpine		
P60-PWR_VGA_CORE (UP1642)	01/04/12		Alpine	No changes from Alpine		
P61-PWR_GPU_DECOUPLING	01/04/12		Alpine	No changes from Alpine		
P62-PWR_+1.5VDDR	01/04/12		Alpine	No changes from Alpine		

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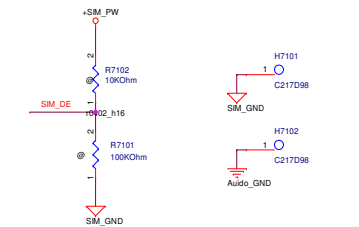
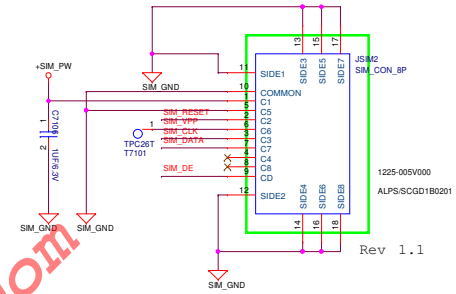
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DWG NO. CORE_B	REV. 2.2	
DATE Thursday, September 18, 2014	SHEET 64 of 65	

		5		4	3	2	1
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	Diago 38 Diago 10	1. Board ID 2. IRQ modify	2014-06-27	Dell Architect	1. Board_ID modify to A02 2. DW1707 can't connection cause IRQ mismatch	1. R392 change to 2kohm 2. HDD_FALL_INT change to IRQC, IRQD reseve for WLAN. Pop R9456 and de-pop R9457	20140627
www.teknisi-indonesia.com							
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						REV. 2.2 SHEET 65 of 65	
		5		4	3	2	1

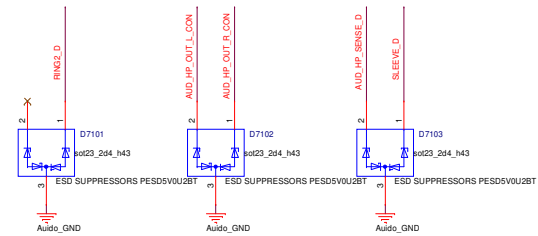
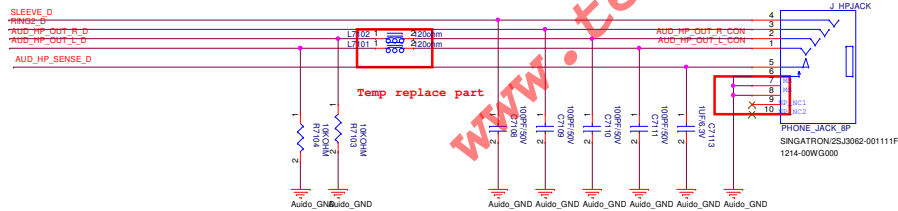
ZIF Connector to MLB



uSIM Card Push-Push



AUDIO COMBO PHONE JACK
auto sense OMTP and CTIA headset / support MIC-IN / HP & mono mic
SLEEVE_D & RING2_D LAYOUT TRACE WIDTH 80 mils

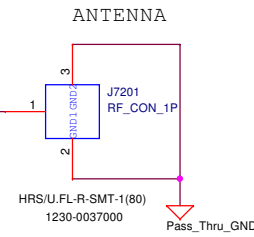
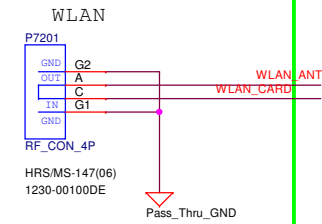


PLACE CLOSE TO J_HP/JACK

Rev 1.1

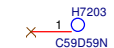
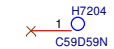
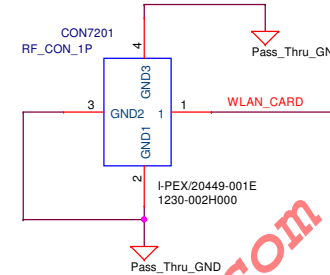
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DWG NO: SIM_B	DATE: Thursday, September 18, 2014	SHEET: 71 of 73	

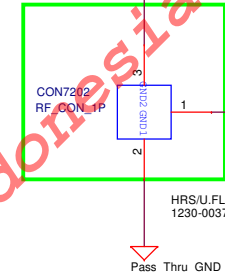
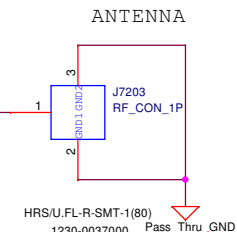
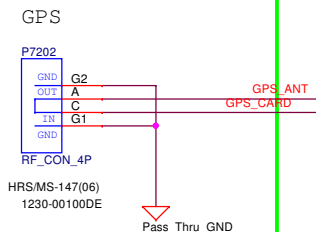


MODULE ANTENNA

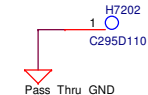
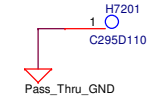
WLAN



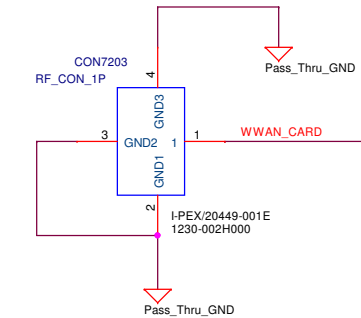
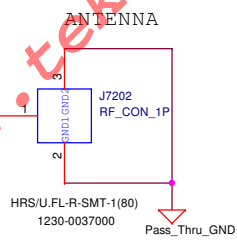
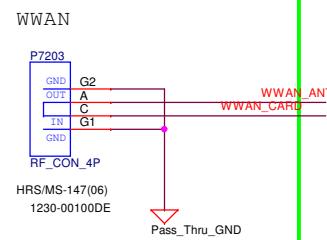
GPS



R1.2 Modify by RF-team to fit the antenna connector



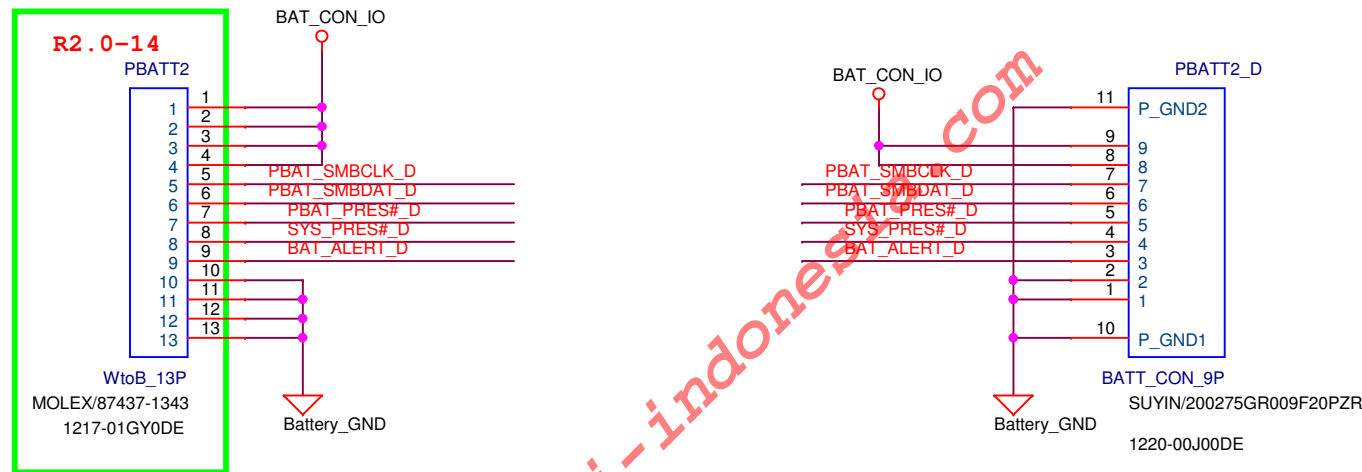
WWAN



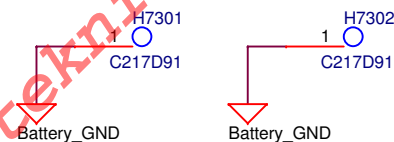
R1.2 Remove the reserved capacitance and resistor by RF-team.

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<p>DWG NO. PASS_THRU_B</p>	<p>REV. 2.2</p>		
<p>DATE Thursday, September 18, 2014</p>	<p>SHEET 72 of 73</p>		



R2.0 Connector pin definition 180-degree rotation



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TITLE BATTERY_B		REV. 2.2	
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